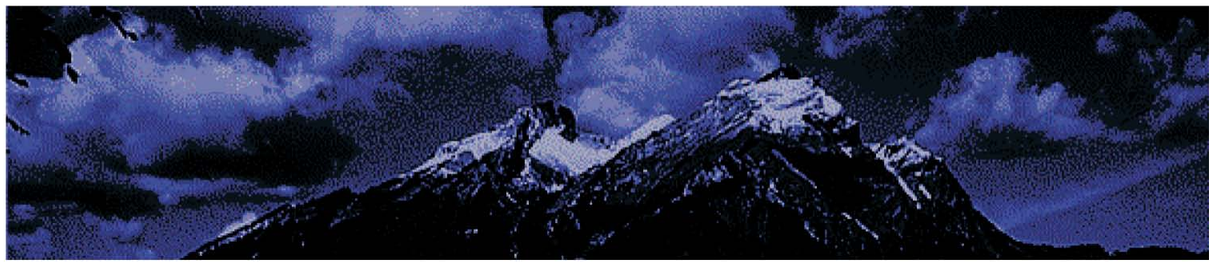

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WOCSDICE 2003

The 27th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe

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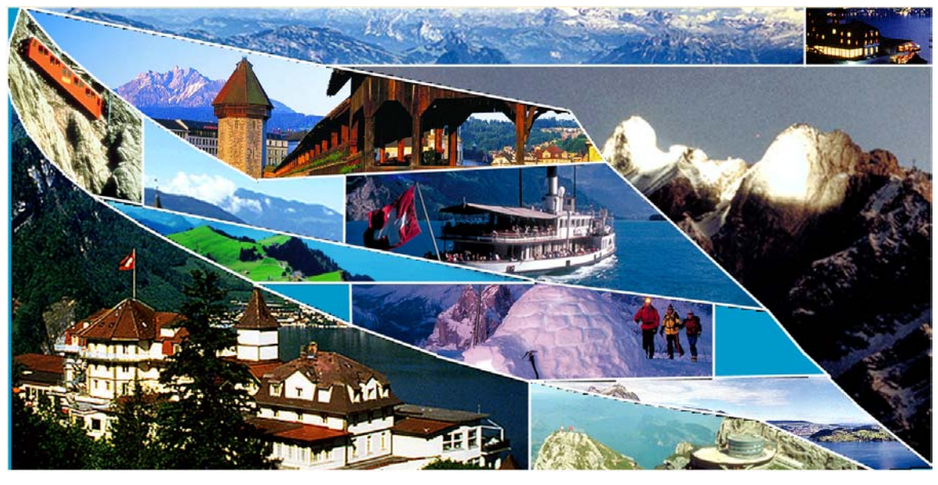

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We wish to thank the following for their contribution to the success of this conference:

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Welcome Address

It is my great pleasure to welcome all participants of the 27th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe, WOCSDICE'03, in Fürigen, Switzerland.

The view to the mountain peaks from this scenic place in the heart of Switzerland has much in common with the idea of the Workshop. Although there are numerous large and small peaks one can only see the most prominent ones on the horizon. In much the same way we hope and we are confident that the conference will display the peaks of worldwide research in the area of Compound Semiconductor Devices and Circuits in microwaves, mm-waves and optics.

Since the first WOCSDICE in 1973 research in compound semiconductors has not lost any attraction and the field as well as the number of specialists has become larger and larger. Although many new conferences on similar subjects have appeared, WOCSDICE has maintained its reputation and its place in the community. It also became a tradition to put particular subjects in the focus of each meeting. In the choice of the invited speakers we have put an emphasis on Gallium-Nitride devices. Subsequently with the incoming proposals for regular papers it became apparent, that this choice is also reflected in a large number of contributions. I am looking forward to an outstanding scientific meeting.

In the organization of this meeting I was particularly fortunate in finding a group of people with experience and dedication and I would like to thank all members of the organizing committee for their cooperation. In particular my thanks go to Annette and Pietro Schicker, who assured me that WOCSDICE had some appeal to them. This workshop will be one of the last in their long-standing conference administration activities.

My sincere thanks also go to the sponsors: (1) the traditional supporters of WOCSDICE, The European Offices of US Aerospace Research and Development, US Army Research Laboratory and US Naval Research, (2) the companies Raith GmbH Dortmund, IBM Research Laboratory, Zürich and CSEM Centre Suisse d'Electronique et de Microtechnique SA, Alpnach with whom we are tied with personal relationships. Thanks to the generous support of these sponsors it is possible to maintain the high standard and the attraction of WOCSDICE.

I am looking forward to interesting scientific sessions, lively discussions, memorable meetings with old and new friends and social get-togethers. For all of this: welcome again and enjoy the stay in Fürigen.

Werner Bächtold
WOCSDICE'03 Chairman

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Recent Advances, Remaining Challenges in Wide Bandgap Semiconductors

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Since the 'second wave' of research into III- nitride and SiC semiconductors in the mid 1980s several 'insurmountable' challenges have been recognized that must be overcome before we can say that they are 'mature' enough for insertion to military applications This paper addresses the most important of these, attempts at their solution, and remaining frustrations.

GALLIUM NITRIDE SUBSTRATES

The extremely high decomposition pressure and melting point of GaN has prevented the development of viable bulk native substrates, by conventional growth methods.

High Pressure Bulk Growth: Grzegory[1] and others have demonstrated ~1 inch square plate-like bulk GaN crystals by spontaneous nucleation in gallium melts under high nitrogen pressures, and temperatures.
They have ~$10^3 cm^{-2}$ dislocation concentrations, but are degenerately n-type (~$10^{20} cm^{-3}$), by a combination of nitrogen vacancies and background oxygen. It is not envisaged that this will become a viable process, as it is difficult to control growth, avoid parasitic nucleation, and introduction of seed crystals.
Such crystals however are useful for research studies where defect densities are important.

Quasi Bulk GaN Substrates: GaN epitaxial films grown at >200μm per hour are under development by Sumitomo and Samsung, and are already commercially available from ATMI and TDI in the USA. They are grown on sapphire, which is subsequently removed by laser treatment at elevated temperatures.
As with most hydrogen-transport growth in quartz reactors, silicon and oxygen background impurities make these 'substrates' n-type with free electron densities usually >5e15cm^{-3}, however Manfra[2] has shown it possible to prepare insulating GaN HVPE by compensation with zinc, after Pankove et al[3].
Dislocation densities decrease from ~1e10 cm^{-2} with the square root of thickness by self-annihilation, so at ~100μm they can be as low as 1e7 cm^{-2}
P-type thick film GaN substrates, for optical diode structure epitaxy, are also available commercially[4]

Quasi Bulk AlGaN Alloy Substrates: Hydride VPE is being used commercially[5] to produce $Al_xGa_{(1-x)}N$ alloy nitride quasi "bulk" substrates for optical device applications.

ALTERNATE SUBSTRATES:

Sapphire substrates are most commonly used for HEMT and other device structure growth, however as noted, above, the ~18% lattice mismatch is responsible for massive interfacial and subsequent threading dislocation density generation.

Silicon Carbide has a good lattice match to AlN, and is used extensively for production of LEDs. A notable advantage is that SiC has a very high thermal conductivity (~3.5 $Wcm^{-1}C^{-1}$). It is not yet readily available in insulating form however, which limits its use for microwave devices. As noted below semi-insulating SIC is soon to be commercially available.
It is still not easy to nucleate nitride films on SiC without using low temperature buffer layers**,** which tend to be degenerately n-type and introduce many extended defects into subsequent epitaxial films. Commercial silicon carbide substrates also suffer from surface, and sub-surface damage.
Ramachandran [6] has shown that this can be removed by hydrogen treatment above 1600C or hydrogen chloride etching ~1100C.

$LiNbO_3$ was recently demonstrated by Doolittle[7] to be a viable alternative to sapphire as a substrate for GaN epitaxy. It is cheaper and available in larger diameters, and possesses many interesting non-linear functional integration possibilities with the semiconducting nitrides.

Lateral Epitaxial Overgrowth (LEO) and Pendeo-Epitaxy

Epitaxial growth through, and laterally over patterned epitaxy-resist masks, such as SiO_2 and SiN_x is found[8] effective in locally reducing the local threading dislocation density in laterally over-grown (LEO) GaN to < $10^4 cm^{-2}$. Large precursor surface diffusion-lengths are a prerequisite however, which limits LEO to HVPE and MOCVD and related growth methods.
Pendeo-epitaxy, a modification of LEO, uses etched pillars of the GaN to nucleate overgrowth and lateral growth. The later has the same order of magnitude defect reduction as LEO does. The 'wings' or laterally overgrown regions also show marked tilt of the crystallographic plane with respect to the substrate of both LEO and PEO films.

"Compliant" Substrates

The concept of defect reduction by introducing compliant strain relieving interface layers between substrate and active layer structure only works for small areas. According to Feng[9] this is because the strain accumulated with increased lateral dimension and layer thickness cannot be accommodated rapidly enough, unless the viscosity of the compliant film is extremely low. (liquid metals, boro-silicate glasses, etc.) and for small

growth rates. In practice compliance is only effective for small areas. It is also labor intensive, requiring etch stop regions or similar 'release' processes for the compliant substrate layer.

Bonding / Smart Cut

Hobart[10] has demonstrated that nitride films can be readily bonded to carrier substrates such as polycrystalline SiC, by growth of epitaxial nitride structures on etch stop films, and subsequent release by etching, ion implantation and thermal treatment, etc. to release the initial substrate. There is much concern over annealing of the damage associated with high doses of helium or hydrogen ions however.

DISLOCATIONS

Scattering and mobility reduction:

As effectively all nitride epitaxial structures are grown on non-native substrates, attention to the electrical and optical effects of associated threading dislocations has received much recent attention. Weimann[11] calculated that low electron mobilities measured in 'bulk' GaN, (subsequently applied to 2D AlGaN/GaN structures) are directly related to dislocation line-lengths, by fixed-charge scattering.

Cai[12] used electron holography to confirm that threading dislocations have typically 1/3 (edge), 2/3-(mixed), and 1 electrons (screw) per lattice-parameter length (in n-type films).

By scanning capacitance microscopy, Smith[13] showed that charge at dislocations come from depletion of film volumes surrounding the dislocations. Thus dislocations can be treated as one-dimensional surfaces with associated mid-gap states.

Work is underway under the Wood-Witt[14] program to elucidate the charge occupancy of dislocations in GaN grown under different stoichiometry and electron and hole concentrations.

Schottky gate leakage and effective barrier height lowering:

Hsu[15] used scanning I-V microscopy to show that many threading dislocations act as leakage paths normal to the surface. The degree of leakage depends on dislocation type as well as growth conditions. Such leakages reduce effective Schottky barrier-heights and increase ideality factors. Furthermore, dislocation-associated gate leakage limits maximum power gain and increases noise in microwave HEMTs

More recently, Miller[16] found that only uncharged dislocations were responsible for anomalous conduction and could be passivated by anodic treatment in aqueous alkaline solution. Leakage currents could be permanently reduced by three orders of magnitude.

P-TYPE CONDUCTIVITY

Magnesium is the only known 'shallow' substitutional acceptor in GaN films. It's effective hole-binding energy at $>10^{20}cm^{-3}$ Mg is > 120meV (>240meV at infinite dilution), which allows maximum hole densities $\sim10^{18}$ cm^{-3}, and makes it thermally unstable, as less than 1% Mg is thermally activated at 300K. Conduction at these impurity concentrations is largely hopping with hole mobilities <10 $cm^2v^{-1}s^{-1}$. This is problematical for npn HBT base-access resistances, and normal conductivity in p-type regions of diode lasers. Ohmic contact resistances are also limited by low hole concentrations.

Superlattice doping: Schubert[17] has used the concept of modulation doping (Mg) in AlGaN/GaN super-lattices to produce $\sim10^{18}$ cm^{-3} quasi-bulk holes with zero thermal-activation energy. Transport normal to the super-lattice planes could be challenge however lateral mobilities were significantly improved over bulk doped GaN.

Dopant free p-type films: Jena[18] recently demonstrated three dimensional electron-gas in graded AlGaN films. Stress-induced piezo-electric fields add to spontaneous polarization to produce distributed electron concentrations.

Mobilities in such impurity free films are thus far higher than in donor–doped films, and limited only by alloy scattering. It is expected that high 3D hole concentrations with two orders of magnitude mobilities will be achieved for use in III-nitride HBTs, and optical diodes.

Polarization Effects,[19] Advantages:

Ohmic contacts: **The** effective barrier to metal contacts has been overcome using the stress induced polarization field imposed by thin GaN/AlGaN near surface heterojunction.

Impurity-free HEMTs

AlGaN capping films on GaN induce piezoelectric charge Asbeck[20], which augments the spontaneous polarization to create 2 dimensional electron gases at the interface. This structure is now universally employed for impurity-free microwave power HEMT channels.

Polarization Effects: Disadvantages

Stark effect: Difficulties in making blue laser diodes have been traced to a combination of factors. The first is the typically high dislocation densities, which act as non-radiative recombination centers. LEO has been employed successfully to reduce the dislocation counts and associated high threshold currents at least over small areas. The oscillator-strength for e-h recombination is also low because of the polarization induced quantum Stark-effect. Narrowing quantum wells in the gain region have reduced this problem, but high carrier effective masses aggravate the oscillator strength by reducing electron / hole wave function overlap. Low hole activation and carrier mobilities also raise series and ohmic contact resistances of p-type layers of diode structures leading to high operating temperatures and increase degradation rates.

Alternate substrate orientations Nitride epitaxial film orientations other than C- (basal) plane are under investigation to obviate the negative (Stark) polarization effects.
Speck[21] recently demonstrated that A-plane GaN will grow on R-plane sapphire, and A-plane silicon carbide. Threading dislocations appear to be lower but textured surface topography is somewhat problematical at the time of writing.
A-plane films are however anisotropic in orthogonal in-plane directions. This property may find application for novel device functional behavior.
Heterojunctions: As there is ~ 4 % lattice mismatch between GaN and AlN, hetero-junctions must be designed carefully to avoid cracking.
It has recently been found that epitaxial heterostructures under tension will form cracks over periods of days or weeks unless processed into smaller areas to reduce the stress accumulated over large areas.
ALUMINUM NITRIDE: Unlike GaN the free energy of reaction of Al with molecular nitrogen according to:

$$2Al + N_2 \; < - > \; 2AlN$$

is negative at the sublimation temperature under atmospheric pressure. As aluminum nitride is naturally insulating, with a very large band-gap it is a good potential substrate for microwave applications.
Bulk growth of AlN by sublimation is thermodynamically viable at ~2300C and will shortly be commercially available in limited diameter wafers[22].
Challenges in cutting and polishing AlN remain however, because of its extreme hardness. Also >3 % mismatch with GaN is a challenge that has yet to be overcome.
INDIUM NITRIDE: Wu and others[23] showed the band gap of InN has recently been found to be 0.7 eV by optical absorption and luminescence of MBE grown films.
This is much lower than the previously published value[24] of 1.8eV, and makes it more interesting for optical applications rather than as a possible alternative to GaN for microwave devices
InN is also extremely difficult to grow as the decomposition temperature is well below the optimum for growth by MOCVD or MBE
SILICON CARBIDE:
Micropipes: Macroscopic holes in SiC substrates (micropipes) are problematical for device performance, as they completely short out high voltage diodes etc. They originate from scratches on seed surfaces, particulates and silicon droplets under poorly controlled temperature and growth stoichiometry.
Better housekeeping and cleanliness as well as purer better controlled source materials and temperature gradient control will eventually reduce micropipes to negligible densities.
Stacking Faults: Bergman[25] first reported the occurrence and propagation of stacking faults in SIC PN diode structures under when driven in forward bias.
Such stacking faults produce 6H quantum wells six atoms pairs wide. Kuhr[26] explained that the activation energy, for sustained propagation of stacking faults, is provided when electrons in the 4H matrix drop into the 6H quantum-well conduction band. There is no apparent solution to this problem except elimination of the dislocations which initiate stacking faults, and the strain which acts as the initial driving force for dislocations to form partials bounding stacking faults.
A and M plane SiC bulk growth: As in the case of GaN epitaxial films, much attention is now being paid to non C-plane oriented bulk[27] and epitaxial[28,29] crystal growth in the USA. Stacking faults are then normal to device carrier trajectories, so not markedly impact the series resistance of high voltage diodes. Poor topography, which negatively impacts device film epitaxial growth, remains an issue on A-plane and M-plane surfaces.
Surface and sub-surface damage: As mentioned above, commercial SiC substrates suffer from residual surface scratches, which propagate into subsequent crystals and epitaxial films as micropipes and dislocations etc. It is up to commercial suppliers to recognize this fact and implement hydrogen polishing or similar damage removal treatments.
Semi-insulating SiC
The extremely high temperatures of growth by physical vapor deposition of bulk SiC enhances the background impurity (usually nitrogen) incorporation leading to n-type crystals.
Vanadium is a compensating deep donor trap in SiC but also produces V-rich inclusions and crystals with non-uniform resistivity distribution. With purer source and graphite container materials, nitrogen exclusion etc. semi-insulating SiC can be prepared by stoichiometry control. SiC is rendered insulating by complexes such as $V_{Si}.C_{Si}$. Under an Air Force 'Title III' program, undoped semi-insulating SiC is now receiving large investment.
Halo-precursor growth: Many residual strains and impurities in silicon carbide crystals stem from the high temperatures used in their preparation (>2200C for bulk, and >1700C for epitaxy) according to:

$$C_2H_4 + 2SiH_4 \; <-> \; 2SiC + 6H_2$$

A new ONR initiative[30] using halo-silane (methane) precursors, together with hydrocarbons (silane), for bulk and epitaxial growth is being investigated to lower bulk and epitaxial growth temperatures by several hundred degrees. It is expected that strain and background impurity incorporation will simultaneously be significantly reduced.

$$C_2H_4 + 2SiH_3Cl \; <- \; H_2 - > \; 2SiC + 4H_2 + 2HCl$$ and similar.

Reductions in bulk SiC crystal growth temperatures to <1600C from ~2200C, and epitaxial growth to < 1100C from ~1700C are possible.
This prediction is supported by the difference between 1100C HCl/H_2 gas polish-etching:

$$SiC + 4HCl \; < - H_2 - > \; SiH_xCl_{(4-x)} + CH_xCl_{(4-x)}$$

vs.1600C for hydrogen alone: $SiC + 4H_2 \; < - H_2 - > \; SiH_4 + CH_4$

In the former case HCl is available for etching high surface energy species, such as silicon droplets, graphite particulates, and islands of mis-oriented SiC etc:

Implantation annealing: Silicon carbide surfaces tend to form large terraces under high temperatures (usually >1800C) required to activate ion implants and remove associated crystal damage.
Such microscopic roughness exaggerates the already very inversion channel electron mobilities of SIC MOSFETs, and complicates lithographic processes.
Aluminum nitride capping layers have recently been shown effective in preventing annealing associated surface roughening, and in maintaining surface stoichiometry.

With continuing efforts supported in large part by the US Office of Naval Research Long-Range Program, it is anticipated that most of these challenges will be met in the near future.
The greatest remaining challenge is that of the electrical activity of extended defects.

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Breakdown and degradation processes in AlGaN/GaN HEMTs during electrostatic discharge

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We study degradation mechanisms in 50 μm gate width/ 0.45 μm length AlGaN/GaN HEMTs under electrical overstresses. 100 ns long rectangular current pulses are applied on the drain contact. Pulsed high current *I-V* characteristics show that after the HEMT undergoes source-drain breakdown (at ~90 V), a negative differential resistance region transits into a holding voltage of ~20 V. Catastrophic HEMT degradation was observed at I_{stress} = 1.65 A due to ohmic contacts burnout. Backside transient interferometric mapping technique reveals a current filament formation in the HEMT channel area.

Introduction

Devices may face electrical overstress (EOS) or electrostatic discharge (ESD) event during manufacturing, handling or device operation [1]. Typical current pulses are in the ampere range with duration between nanoseconds and microseconds. The importance of failure mechanism study in III-nitride transistors is given by their potential usage in defense and commercial applications where harsh conditions can be expected. Current conduction mechanism in GaAs-based HEMTs during high current source-drain pulses was analyzed by Vashchenko et.al. [2]. Parasitic bipolar effect driven by an avalanche-injection process have been found to be responsible for the negative differential conductance in the high-current *I-V* characteristics. Critical issue is that the electrical breakdown in the transistor buffer layer is accompanied by high current density filament formation with possible thermal run-away and device failure. In this work dc and optical characterization methods are used to follow the evolution of degradation processes in overstressed AlGaN/GaN HEMTs. Parameters of the gate and source/drain contacts together with parameters that are related to AlGaN/GaN quantum well properties are investigated to specify the cause of the device failure. Optical thermal mapping experiments are used to clarify the relation between electrical and thermal processes.

Experiment

The AlGaN/GaN HEMT structures used in this study were grown on 330 μm thick both-sides polished sapphire wafers by MO-VPE. Device processing was described elsewhere [3]. 100 ns long rectangular pulses using a transmission line pulser are applied on the drain contact keeping the source grounded and gate floating. The current and voltage waveforms were recorded using a digital oscilloscope and *I-V* characteristics were extracted using averaged values over the time span from 85 to 90 ns. Devices were dc characterized after consecutive current stresses. Gate-source *I-V* characteristics were measured to evaluate *Schottky* contact degradation, while *ohmic* contact and open channel resistances were extracted using the dc method [4]. This, together with threshold voltage values was used to determine degradation processes. We used backside laser

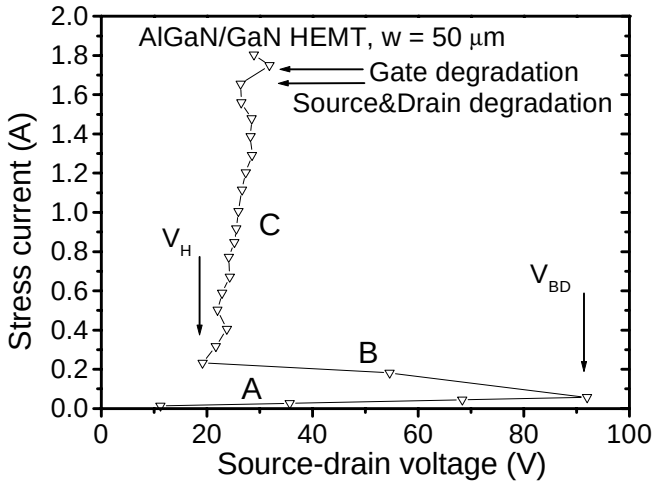

Fig.1 HEMT pulsed *I-V* characteristic

beam interferometric mapping technique [5] to localize current path in HEMTs during TLP stresses. The measured phase shift, caused by the temperature-induced change in the refractive index, is directly proportional to a local 2D energy density in the device.

Results

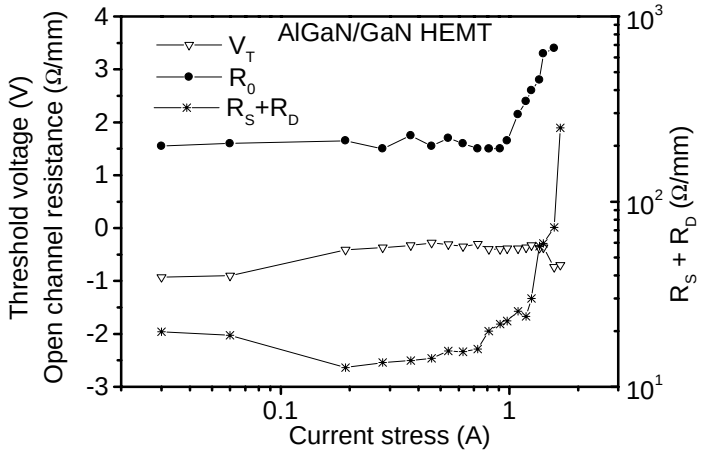

Fig.2 Evolution of the HEMT dc parameters

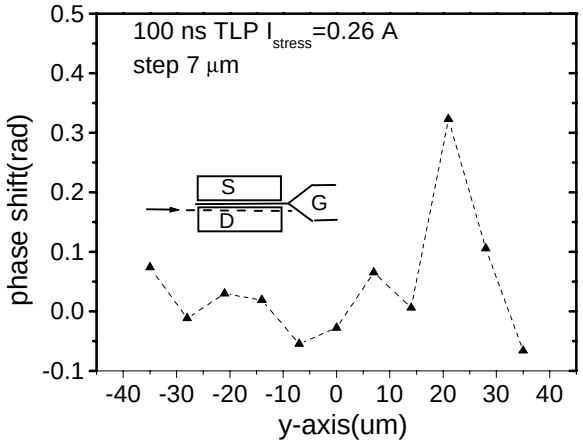

Fig. 3 Distribution of phase shift along the HEMT

The pulsed *I-V* characteristic (Fig.1) showed three regions: the low current/ high voltage region A, the negative differential conductivity (NDC) region B, and the high-current/low voltage region C. Evolution of the HEMT *Schottky* contact characteristics (not shown) after particular current stresses indicates that the gate remains functional up to I_{stress} = 1.75 A. The transistor threshold voltage V_T, open channel resistance R_0, and the sum of the source R_S and drain R_D *ohmic* contact resistances as a function of the current stress level are shown in Fig. 2. At I_{stress} = 0.2 A (onset of NDC, Fig.1) a shift of the threshold voltage upwards, from the nominal value of V_T = –0.9 V to the value of V_T = ~ -0.4 V can be observed. If one considers constant QW equilibrium carrier density (as indicated by constant R_0 for I_{stress} < 1 A) this effect can be explained by the electron trapping in the device buffer layer and consecutive channel depletion from the back side. The *ohmic* contacts catastrophic degradation (ten-fold increase from the nominal value) was recorded at I_{stress} = 1.65 A. Fig. 3 shows the phase shift (i.e. current) distribution as a function of position along the device width. The device was scanned along the drain at I_{stress} = 0.26 A (region C, Fig.1). A phase peak is found at the right edge of the HEMT channel, indicating the current filamentation.

Conclusion

The interferometric technique and the HEMT dc characterization show that the NDC region of the pulsed *I-V* characteristic is linked to the current filamentation in the device buffer. The *ohmic* contact degradation terminates the HEMT functionality after the EOS/ESD event at I_{stress} = 1.65 A.

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The Temperature Dependence of Impact Ionisation in Semiconductors

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The temperature dependence of breakdown voltage is examined in GaAs and $Al_{0.8}Ga_{0.2}As$ and compared with Si, SiC and GaN data from the literature. Of the materials considered it is shown that GaN shows the greatest variation in breakdown voltage with temperature. The differences shown are explained in terms of differing ionisation threshold softness.

Introduction

Impact ionisation is the process in which a carrier that has been accelerated to a high energy by an electric field, imparts its energy to a bound carrier to create a secondary electron hole pair. This process results in avalanche multiplication of charge carriers that limits the operating power of transistor devices and also provides current gain in Avalanche Photodiodes. Impact ionisation is temperature sensitive owing to the dependence of carrier cooling by phonon scattering on the phonon population, *n*, which in turn varies as

$$n = \frac{1}{1 - \exp\left(\frac{\hbar\omega}{kT}\right)}. \qquad (1)$$

Here $\hbar\omega$ is the phonon energy, *k* is Boltzmann's constant and *T* is the absolute temperature. The temperature dependence of impact ionisation has been studied in a number of materials including Si [1], GaAs, $Al_{0.6}Ga_{0.4}As$ [2], 4H-SiC [3] and GaN [4]. In this Letter we report experimental breakdown voltage data as a function of temperature for GaAs and $Al_{0.8}Ga_{0.2}As$ p^+in^+ diodes compared with data taken from the literature for a range of semiconductors in an attempt to understand their temperature dependent behaviour.

Experiment

A series of GaAs and $Al_{0.8}Ga_{0.2}As$ p^+in^+ diodes were grown by MBE and etched into mesas using standard wet chemical etching. The i-region width was estimated by CV measurements to be close to the nominal width of w=1μm in all cases. The breakdown voltage, V_{bd} was determined by reverse IV and photomultiplication measurements at temperatures between 20K and 290K performed in a He cryostat. V_{bd} is defined as the voltage for which the current increases by more than an order of magnitude in a 100mV step. Typical IV characteristics as a function of temperature for a w=1μm GaAs p^+in^+ diodes are shown in Figure 1. It can be seen that dark current is low and breakdown is sharp in all cases.

The results are shown in Figure 2 together with calculated characteristics from ionisation coefficients for Si [1] and experimental results for 4H-SiC [3] and GaN [4] taken from the literature. An appropriate built in voltage is included for all the characteristics shown. As can be seen all materials show a positive temperature dependence of breakdown voltage, in accordance with equation 1.

Discussion

To make a meaningful comparison between the materials shown, we must first deconvolve the effect of differing device widths. It has been shown by Harrison *et al.* [3] that for the high fields present in thin devices, the temperature dependence of impact ionisation is reduced as carriers undergo fewer scattering events with phonons in their correspondingly shorter

ionisation path lengths. The device widths of the Si, $Al_{0.8}Ga_{0.2}As$ and GaAs devices are all w=1μm whereas the GaN and SiC devices are w=0.25μm and w=0.4μm respectively. Therefore, the SiC and GaN may show greater variation in V_{bd} with temperature if they were the same thickness as the other devices.

Figure 2 shows that GaN shows a much larger variation in breakdown voltage with temperature than SiC, which is noteworthy due to the high power applications of these materials. Figure 2 also shows that there is no clear trend relating temperature variability in breakdown voltage with bandgap of the host material.

Here we argue that the differences in temperature behaviour are due to the differences in ionisation scattering rate softness, i.e. how slowly the ionisation scattering rate rises with energy. This can be understood as follows. The distribution of the carriers in energy depends on temperature via the phonon scattering rate. This determines the ionisation rate sampled by the carrier distribution and hence the ionisation coefficient. Materials with softer ionisation thresholds will be less temperature dependent than materials with harder thresholds, simply because heating or cooling the carrier distribution will cause a smaller change in the ionisation rate sampled. This hypothesis supports the results shown, as both Si and $Al_{0.8}Ga_{0.2}As$ are thought to have a softer ionisation threshold than GaAs [5]. Data is not available for SiC and GaN to see if these materials also follow this trend.

Conclusions

It has been shown that the temperature dependence of V_{bd} in diodes varies significantly with host material. Interestingly, GaN shows the greatest variation in spite of its wide bandgap. The temperature dependence of breakdown voltage appears instead to be due to differences in the ionisation threshold softness.

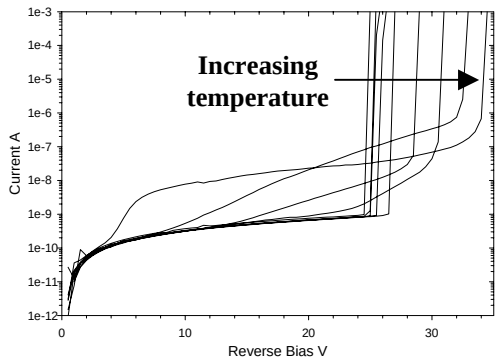

Figure 1: Reverse IV characteristic for a w=1μm GaAs p^+in^+ diode at temperatures between 20K and 290K

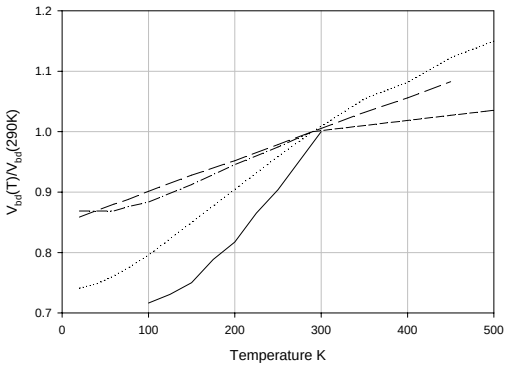

Figure 2: $V_{bd,}$ normalised to the 290K value, for a series of diodes comprised of Si (long dash), GaAs (dotted), AlGaAs (dot-dashed), SiC (short dash) and GaN (solid)

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Characterization of near-surface inhomogeneities in GaN epilayers by DLTS and EBIC

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Electrically active defects in Schottky barrier structures formed on n-GaN layers are investigated by the deep level transient spectroscopy and electron beam induced current techniques. Examples of depth and lateral inhomogeneity characterization are presented. The efficiency of combined application of both mentioned techniques is demonstrated.

Introduction

Electrical parameters of GaN-based devices such as breakdown voltage and leakage current are essentially influenced by properties of near-surface regions and lateral inhomogeneities of epitaxial layers. To clarify reasons and an origin of this influence the study of the relation between layer inhomogeneities and electrically active defects is required. Energetic parameters of electrically active centers and their depth distribution are used to be characterized by the Deep Level (DL) Transient Spectroscopy (DLTS) and capacitance-voltage technique, while the lateral distribution of electrically inhomogeneous regions could be revealed by the Electron Beam Induced Current (EBIC) technique. In recent studies [1,2], it was shown that in GaN layers the diffusion length could be about a few tenths of micron that allows to obtain EBIC images with unexpectedly high lateral resolution so that even individual extended defects could be observed. A lateral distribution of point defects determining the excess carrier recombination rate also could be characterized by the local value of diffusion length with the high resolution. Thus, combined application of the EBIC and DLTS techniques is expected to be a promising tool for the study of inhomogeneities in GaN layers.

Results and discussion

In the present work, several types of n-GaN epitaxial layers grown by metal-organic chemical vapor deposition (MOCVD) with different buffer layer conditions on sapphire substrates have been studied by the DLTS and EBIC. A thickness of layers is about 3 μm and carrier concentration is found to be of $(1\text{-}20)\times10^{16}$ cm^{-3}. The dislocation density in different samples is varied in the range from 10^8 to 10^9 cm^{-2}. For electrical measurements Au/Ni/n-GaN Schottky diodes with the area of 0.19 mm^2 have been prepared.

Two interesting results concerning depth and lateral inhomogeneities of electrical properties of GaN layers are obtained. It is found that the DLTS spectra in the bulk of the layer and near the metal-semiconductor interface are different for all types of samples. In addition to the DL commonly observed in MOCVD-grown GaN [3-5], a new feature in the DLTS spectra at 200-250 K is found in near-surface region (Fig.1). The observed wide peak E_{sf} corresponds to, at least, two DL defects

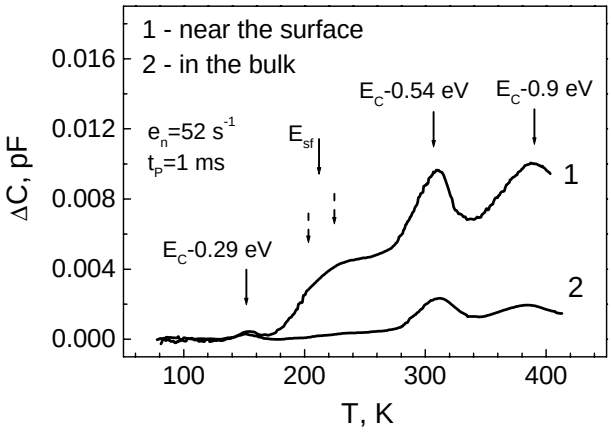

Fig. 1. Typical DLTS spectra in near-surface region and in the bulk of GaN layer

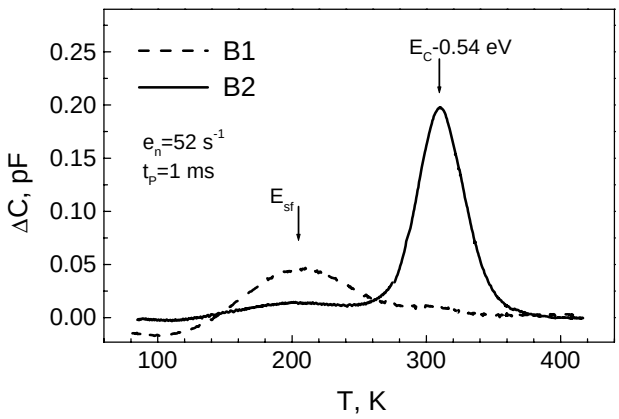

Fig. 2. DLTS spectra in two diodes (B1 and B2) with different DL concentrations from the same sample.

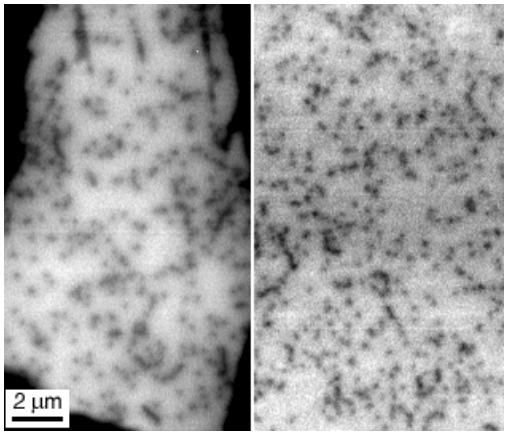

Fig. 3. EBIC images obtained on the diodes B1 and B2 under the same measurement conditions.

located at the depth less then 0.1 μm from the GaN surface. Earlier, the existence of unintentionally induced donors with the energy level about E_C-0.4 eV near a metal-semiconductor interface, which are responsible for large leakage currents in GaN-based Schottky structures, was concluded by Hasegawa *et al* [6] from current-voltage characteristic analysis. The estimated parameters of the DL defects observed by DLTS are close to those predicted in [6].

To study the lateral inhomogeneities and to find a correlation between the defects revealed by the DLTS and EBIC, the data obtained on different samples and on the diodes with different DL concentration on the same sample have been compared. It is found that the concentration of the most prominent trap E_C-0.54 eV correlates with the density of extended defects (dislocations) both for different samples and for the diodes on the same sample. The EBIC detects also that a minority-carrier diffusion length is lower in the diodes with the higher concentration of trap E_C-0.54 eV. In addition, it is found from fitting the dislocation EBIC profile that the average diffusion length is determined not by dislocations but probably by point defects, although the concentration of these defects was shown [2] to increase with the increase of extended defect density. As an example, the DLTS spectra and typical EBIC images for the diodes B1 and B2 from the same sample are presented on Fig. 2 and 3, respectively, the concentration of DL defects E_C-0.54 eV in diode B2 being tens times higher than that in B1.

Thus, the DL E_C-0.54 eV could be associated either with extended defects or with point defects determining the diffusion length. An analysis of capture kinetics for trap E_C-0.54, in particular, the DLTS peak amplitude on filling pulse dependences, does not allow to choose definitely between these two possibilities since the dependences obtained are rather complicated and require further investigations, probably, using mathematical simulation with various models for DL defect localization.

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Photoconduction in Porous GaN/SiC Structures

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Photoresponse is studied in porous GaN/SiC samples fabricated by surface anodization of structures comprising epitaxial GaN layers and 6H-SiC substrates, on which the layers were grown. It is shown that the photoresponse signal originates at the interfaces in the anodized GaN/SiC structure, and its characteristics are similar to those of GaN samples demonstrating persistent photoconductivity (PPC) effect. The features of the porous GaN/SiC structure make it a suitable object for studying the validity of the model stating that PPC in GaN is likely to be due to light-induced modulation of space charge regions around the defects present in the material.

Introduction

Gallium nitride is a very promising material for fabrication of ultraviolet photodetectors [1]. Unfortunately, GaN-based photoconductors suffer from the presence of persistent photoconductivity (PPC) effect. Their photoresponse is characterized by very long build-up and decay times, which make them hardly suitable for practical applications. A number of models has been proposed to explain the PPC effect, and recently, Garrido *et al*. suggested that PPC in GaN is due to the conduction modulation rather than a conductivity one [2]. According to [2], Space Charge Regions (SCR) inside the semiconductor are modified by the incident light and determine the conductance in the sample. These SCR are presumed to be located at the defect areas such as grain boundaries, dislocations [2], or at the epitaxial layer/substrate interface [3]. This model has been successfully employed to describe PPC effect in GaN and AlGaN [1] and similar considerations have been used to explain transport properties of GaN layers [4]. This suggests that PPC effect can be in principle eliminated in a very high-quality GaN material, but further proofs for the model are needed.
Porous GaN and SiC in this respect are very interesting objects since they possess large internal surface area, which is likely to hold surface states surrounded by SCR. Recently, it has been suggested that it is the SCR of surface states on the pore walls that determine the effective density of carriers in porous SiC [5]. It has been already shown that the unique properties of porous SiC can make them ‘model objects’ for in-depth physical studies [6]. Photoresponse studies in porous GaN/SiC structures represent a great interest in this respect, as they may help fighting PPC effect in real GaN-based photodetectors.
In this work, we report on the photoresponse studies in porous GaN/SiC structures. Photoresponse was studied at 300 K and a strong photoconduction was observed in porous GaN/SiC structures, whereas no photoconduction in non-anodized structures or in anodized SiC substrates was detected. The photoresponse in the anodized samples is ascribed to the SCR of the states located at interfaces in porous GaN/SiC, thus supporting the model of [2].

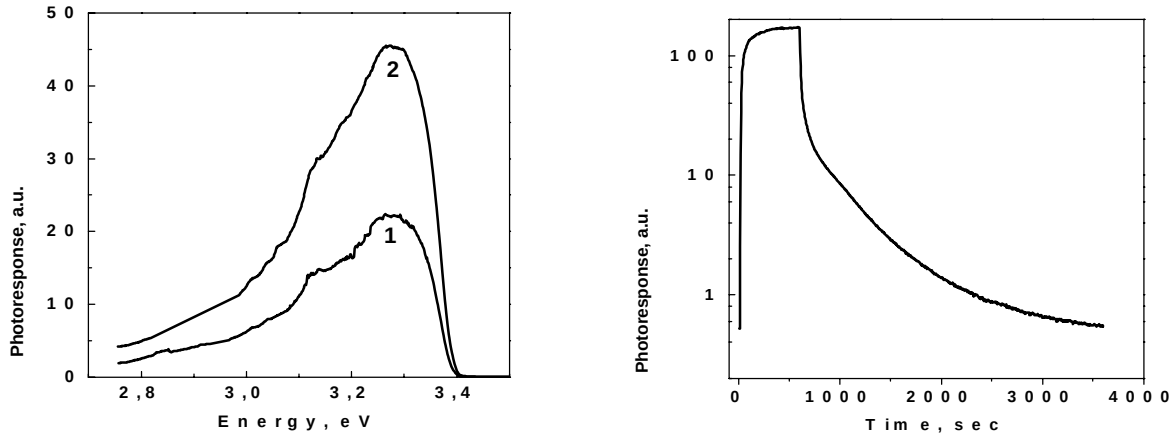
Results and Discussion

Initial GaN/SiC structures consisted of thin (0.3-0.6 μm-thick) epitaxial n-type GaN layers and 6H-SiC substrates. The structures were anodized in aqueous solution of HF as described elsewhere [7]. As a result of anodization, a several μm-thick porous layer was formed, which comprised both a porous GaN layer and a porous layer in the SiC substrate.
Photoresponse measurements were performed with excitation by a broad spectra light source in ac (modulation by a chopper with frequency variation) and dc mode. The kinetics of the photoresponse was studied in dc mode. The dc photoresponse spectra of two structures from

the same initial GaN/SiC sample anodized under 10 (curve 1) and 20 (curve 2) mA/cm^2 current density, respectively, are presented in Fig. 1. As can be seen, photoresponse was observed only for photons with energy below the GaN bandgap. The spectra are similar in shape with photoresponse increasing with anodization current.

Fig. 2 shows build-up and decay of the photoresponse from the porous GaN/SiC structure, obtained by anodization at 20 mA/cm^2 current density. Photoresponse was excited at 375 nm wavelength. As can be seen, the decay could not be fitted with a single exponential function and the observed characteristic times (hundreds and thousand of seconds) are typical for PPC in GaN reported in the literature. Similar non-exponential curves were observed for the build-up and decay of dark currents in the studied structures under applied voltage.

The data obtained generally correspond to the characteristics of PPC in GaN used for developing model of Ref. [2], so the photoconduction must be due to the SCR areas present in the sample. Since no photoresponse was observed in porous SiC substrates, most likely that it was the interface between the porous GaN and porous SiC developed under anodization that was responsible for photoconduction. To clarify this matter, additional characterization of the structures was performed. Photoluminescence studies showed a little difference between the



spectra of initial and anodized structures. At the same time, Scanning Electron Microscopy in Electron Beam Induced Current (EBIC) mode showed a drastic increase of the potential barrier height at the GaN/SiC interface after anodization. Since the results of both Raman scattering and Schottky diode C-V measurements did not reveal any drastic changes in carrier concentration in GaN after anodization, the increase in barrier height could be attributed to the changes at the interface. Also, a large density of charged states has been detected by EBIC at the interface between the porous SiC layer and the crystalline part of the SiC substrate in the structure, so possible contribution of these states to the photoconduction is discussed as well. We believe that the concentration of surface states at the formed interfaces far exceeds that in the 'bulk' of porous GaN and SiC, so the contribution of SCR of the states located on pore walls is not observed. Thus, generally our results support the validity of the model of PPC in GaN developed in Ref. [2], and confirm the idea that porous GaN and SiC can be used as model objects for studying various physical effects in wide band-gap semiconductors.

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Effect of SiN_x passivation on surface and interface charge instability in AlGaN/GaN heterostructures and HFETs

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Large instability in surface and interface charges in unpassivated AlGaN/GaN heterostructures has been observed under different perturbations. Exposure to UV illumination results in large reduction of the net surface and interface sheet charge density as inferred from the large reduction in surface barrier. On the other hand, stressing by high negative bias on the gate and positive bias on the drain of a transistor results in an increase in the net sheet charge concentration across the AlGaN barrier layer as indicated by a large increase in surface barrier near the gate. After SiN_x passivation the surface and interface charges stabilize to a large extent.

Introduction-Design-Experimental Verification

There has been considerable research interest in III-Nitrides in the past few years in part due to their applications in high power microwave devices. The AlGaN/GaN heterostructure grown on sapphire or SiC substrate, which has been widely accepted for fabricating microwave heterostructure field effect transistors (HFETs), forms a two-dimensional electron gas (2DEG) at the interface without any intentional doping due to its polarization properties [1]. However the 2DEG concentration at the interface is dependent on the electric field in the AlGaN barrier, which in turn is controlled by the surface barrier height. In this paper, we will discuss the instability of surface and interface charges for unpassivated AlGaN/GaN heterostructures and HFETs, studied by UV laser illumination and bias stress and the effect of SiN_x passivation on such instability.

The experimental conditions for the respective cases have been described in detail earlier [2 – 4]. AlGaN/GaN heteostructures before and after SiN_x passivation were exposed to UV illumination, and the result is shown in Fig 1 (a) and (b). As can be seen from the Fig 1 (a), before passivation the surface barrier changed a lot (~0.7 eV) under UV illumination. However, after passivation the change in surface barrier is much less ~0.1 eV. Thus the fluctuation in surface and interface charge density was minimized after passivation. On the other hand unpassivated HFETs showed large changes in surface potential near the gate after stressed under high gate and drain biases, as opposed to passivated HFETs that shows much lower changes [see Fig. 2(a) and (b)]. These experimental evidences indicate that the surface and interface charges are stabilized to a large extent after SiN_x passivation. The exact reason for such stabilization has not been established as yet. However, there are some indications that charges in SiN_x (which is non-stoichiometric) might be responsible.

Conclusions

In conclusion, we have studied the charge instability in unpassivated AlGaN/GaN heterostructures and HFETs. We have found that before SiN_x passivation, the surface and interface charges can be changed to a large extent by external perturbations. However, after passivaion the surface and interface charges are stabilized and cannot be easily perturbed.

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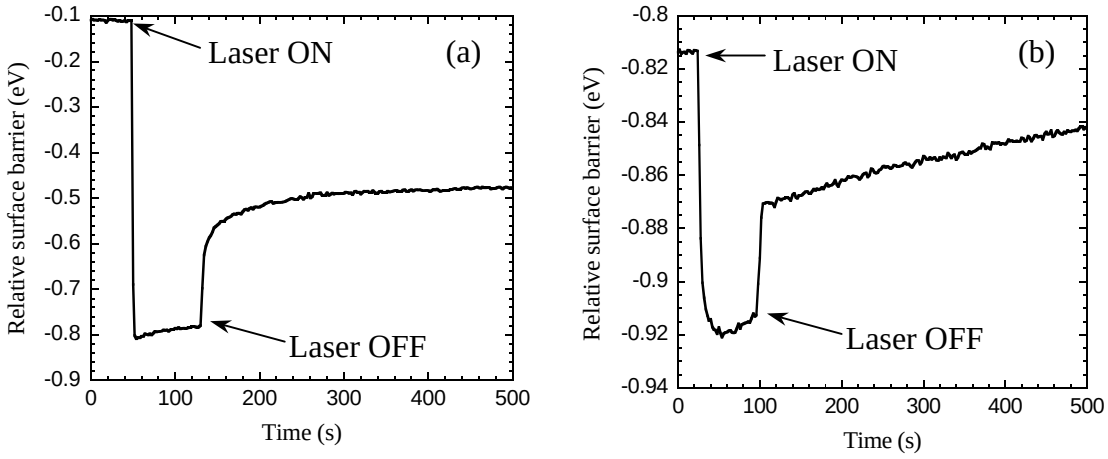

Fig. 1 Surface barrier transients caused by switching an UV laser ON and OFF for an (a) unpassivated and (b) SiN_x passivated AlGaN/GaN heterostructure (35% Al, 250 Å barrier thickness) grown on Sapphire.

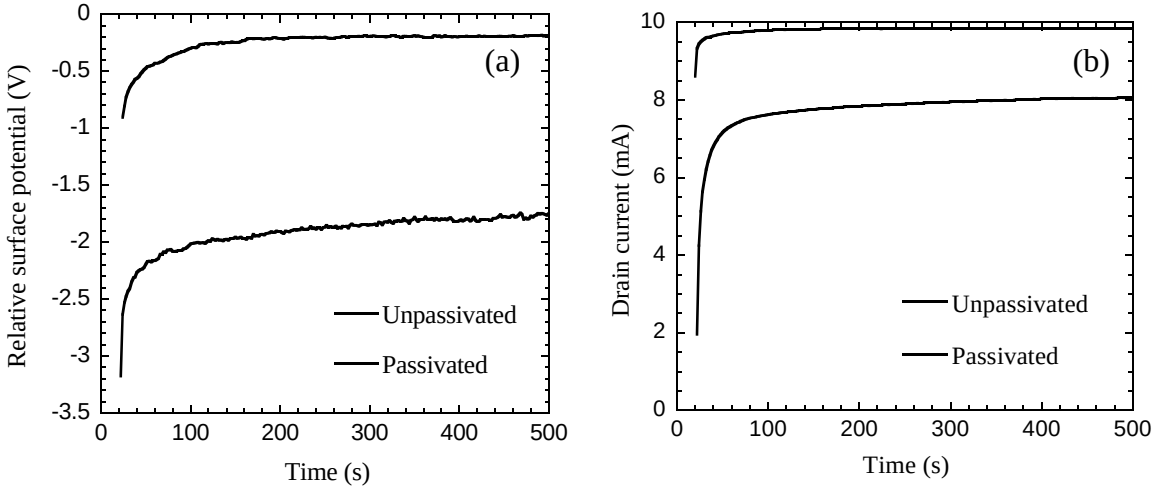

Fig. 2 Comparison of the (a) drain current and (b) surface potential recovery transients before and after passivation for a 100 μm wide AlGaN/GaN HFET device. Before measurements the device was stressed at V_d = 20 V, V_g = -12 V for 2 mins, while during measurement, V_d = 1 V, V_g = 0 V.

Growth of High Quality AlGaN/GaN HEMTs by PA-MBE on MOCVD GaN Templates

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This work reports on the influence of the MOCVD GaN templates on the quality of the MBE-grown AlGaN/GaN heterostructures. Detailed optical and structural characterization results show that the residual compressive strain and the crystalline quality of the MBE heterostructures mimic those from the templates used. Our comparative study shows that when high quality GaN templates are used, AlGaN/GaN HEMTs grown by MBE have similar performances as the ones fully grown by MOCVD.

Introduction. In the past ten years there has been a remarkable progress in the AlGaN/GaN material quality, and, subsequently in the process to convert these structures into efficient high power microwave transistors [1]. Actually, one of the main limitations is the lack of commercial nitrides bulk substrates. The MBE technique has demonstrated its effectiveness and advantages to produce high quality AlGaN/GaN heterostructures [2-3]. MBE growth on sapphire or SiC substrates, using an AlN buffer layer, generally yields nitride layers with lower crystalline quality than MOCVD material, most likely due to the strong growth temperature difference that results in larger grain size and low defect density for MOCVD. Therefore, an effective approach to use MBE is to grow "quasi" homoepitaxially on GaN templates grown by MOCVD on sapphire.

Experimental. AlGaN/GaN heterojunctions were grown by plasma-assisted MBE (PA-MBE) under Ga-stable conditions on semi-insulating MOCVD GaN-templates on c-plane Al_2O_3. We have used templates from three different sources (labelled as A, B and C). The MBE-grown layer structure consists of a 1μm thick GaN layer followed by an undoped AlGaN barrier with Al compositions ranging from 26% to 32% and thicknesses from 15 to 40 nm. The AlGaN/GaN heterojunctions were characterized by photoluminescence (PL), high-resolution X-ray diffraction (HRXRD) under symmetric (00.2) and asymmetric (±10.5) reflections, capacitance-voltage (CV), and Hall effect measurements. MBE- and MOCVD-grown HEMTs were processed and characterized under DC and RF operation.

Results and Discussion. Low temperature PL spectra reveal similar emissions from GaN layers, either that from the MBE-grown AlGaN/GaN heterostructure, or that from the template. The dominant free and donor-bound exciton peaks reveal their high crystal quality. All spectra are blue-shifted from the energy corresponding to fully relaxed GaN, as it is expected from the growth of GaN on sapphire (compressive biaxial stress). Strain differences observed between the GaN MBE-grown layers, estimated from a linear variation of the free exciton-A energy with strain [4] (Fig. 1a), can be attributed to changes in the growth conditions of the MOCVD templates used. The full width at half maximum (FWHM) of the HRXRD rocking curves gives

information on the crystal quality, being quite similar for the MBE-grown GaN in the AlGaN/GaN heteroestructures and the GaN from the templates.

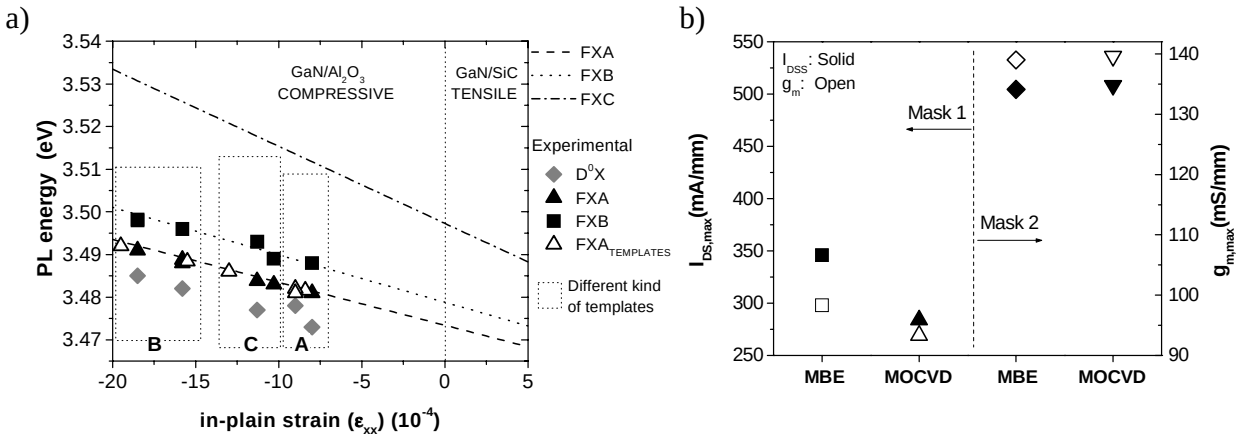

Fig. 1 (a). Position of the dominant PL emission at 9K versus the biaxial strain for: i) the GaN epilayer from the MBE AlGaN/GaN heteroestructures (solid symbols); ii) the GaN template (open triangles); and iii) linear variation of the free exciton from Shan et al. [4] (lines). (b) Average $I_{DS,max}$ (solid) and $g_{m,max}$ (open symbols) from MBE- and MOCVD-grown HEMTs, with L_G=2μm y W_G=300 μm, processed with two different mask-layouts.

On the other hand, a comparative study of device characteristics fabricated from AlGaN/GaN heterostructures grown either by MBE (three samples) or by MOCVD (three samples) is also presented, showing similar performances in $I_{DS,max}$, $g_{m,max}$, f_T and f_{max}. Average values of $I_{DS,max}$ and $g_{m,max}$ are shown in Fig1b. The average f_T and f_{max} (not shown here) are respectively 4 and 12 GHz for MBE devices, and 4 and 9 GHz for fully MOCVD devices, with L_G=2μm and W_G=300μm, processed with the optimized mask (Mask 2).

Conclusions. This work shows the influence of the GaN template quality on the MBE-grown epilayers. The residual strain and crystalline quality are inherited from the template, thus it could be a limitation for high quality MBE structures. However, for high quality templates HEMT devices grown by MBE are as efficient as those fully grown by MOCVD, in terms of I_{DS}, g_m, f_t and f_{max}.

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Intersubband-Photodetector at 1.55 µm using a GaN/AlN-Superlattice

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Abstract

We report optical absorption and photocurrent measurements on a GaN/AlN-based superlattice. The optical absorption has a full width at half maximum (FWHM) of 120 meV and takes place at an energy of 660 meV (5270 cm^{-1}); this corresponds to a wavelength of 1.9 µm. While the optical absorption remained unchanged up to room temperature, the photocurrent signal could be observed up to 170 K. With respect to the optical absorption, the position of the photocurrent peak was slightly blue-shifted (710 meV / 5670 cm^{-1}) and had a narrower width of 115 meV. Using this near-infrared quantum well infrared photodetector (QWIP), we were able to measure the spectrum of a 1.55 µm superluminescent light emitting diode (SLED).

Introduction

Optical devices based on intersubband transitions have seen a decade of tremendous progress which led, among other milestones, to the demonstration of high performance quantum cascade (QC) lasers [1], and highly sensitive infrared cameras based on arrays of QWIPs [2]. For telecommunication applications, there exist basically two different possibilities: one can either work in one of the atmospheric window regions and utilize, for instance, standard 10 µm QC lasers in conjunction with QWIPs or classical mercury-cadmium-telluride detectors; or use 1.55 µm interband lasers and detect the radiation with fast interband or intersubband detectors at these near-infrared (near-IR) wavelengths. Since its conduction band discontinuity is on the order of 2 eV, the material combination AlN/GaN is the ideal material system for such near-IR intersubband detectors. In this article, we thus present results on a GaN/AlN-based QWIP working at wavelengths down to 1.55 µm.

Experimental Set-up and Results

Growth of these superlattices was based on molecular beam epitaxy on c-face sapphire substrates. After a very thin AlN nucleation layer, a 500 nm thick n-doped (Si, 5 x 10^{18} cm^{-3}) $Al_{0.5}Ga_{0.5}N$ buffer layer was grown, followed by a 20 period GaN/AlN superlattice with 20 Å thickness for each layer and n-doped wells (Si, nominally 5 x 10^{19} cm^{-3} to 10^{20} cm^{-3}). The top layer was a 100 nm thick n-doped (Si, 1.5 x 10^{18} cm^{-3}) $Al_{0.5}Ga_{0.5}N$ layer. After growth, the samples were metalized using a shadow mask with 800 µm wide openings. We first deposited a Ti/Al/Ti/Au (40/2000/40/2000 Å) ohmic contact which was annealed at 800 °C for 60 s. Between the annealed ohmic contact stripes, we evaporated stripe-shaped Pd/Au (40/2000 Å) Schottky contacts. The wafer was then polished in a standard multi-pass waveguide geometry with two parallel 45 ° wedges and a polished back (see inset of figure 1). Using a small In dot which was squashed towards the polished edge of the wafer, we connected the ohmic top contact - and probably also the underlying superlattice and the buffer layer - to the copper submount, whereas the Schottky contact was bonded to an Au-coated ceramic contact pad. Due to the rather low lateral conductivity of the top contact layer, the superlattice was not short-circuited by the In dot.

In figure 1, we present a computed band diagram of our structure. The conduction band discontinuity was assumed to be 2.1 eV. All layer thicknesses are 20 Å, and the internal fields at each interface are +-6.5 MV/cm. The simulation was done assuming a superlattice with an infinite number of periods, no boundary effects, and no external bias voltage. Based on these assumptions, we found a transition energy of 610 meV between the first excited state and the ground state. Optical absorption curves were

obtained from transmission measurements under both polarizations, and subsequent normalization using the formula $\alpha L = \mathrm{Log}(T_{TE}/T_{TM})$. T_{TE} and T_{TM} are the transmitted intensities in the two polarizations, and αL is the absorbance of the structure. From the integral under the absorbance curves, we deduced a carrier density of 6.5 x 10^{19} cm^{-3}; this value is consistent with the intentional doping level in the wells. The absorption signal peaked at 5270 cm^{-1} (660 meV / 1.9 µm) and showed a FWHM of 120 meV. As expected, the TM photocurrent signal was slightly blue-shifted with respect to the absorption, peaked at 5670 cm^{-1} (710 meV / 1.76 µm) and had a FWHM of 115 meV.

In order to obtain the responsivity of this QWIP, we replaced the internal white-light source of the spectrometer by a narrow emission 1.55 µm SLED. In figure 2, we present several photocurrent measurements as a function of temperature using the white-light source; and one curve showing the emission spectrum of the SLED. Based on these measurements, we found a responsivity of 100 µA/W, and a detectivity of 2 x 10^9 $(cm^2 \times Hz)^{1/2}/W$.

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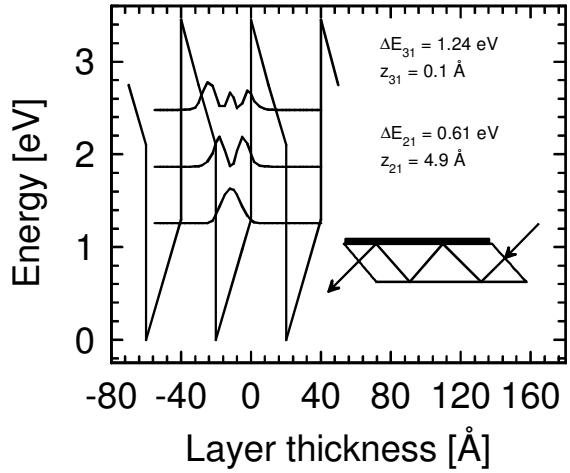

Fig. 1 - Schematic conduction band structure of a GaN/AlN superlattice with 20 Å thick well and barrier layers. The observed transition, ΔE_{21}, takes place between the ground state and the first excited state and has a computed energy of 610 meV. The inset shows a schematic cross-section through the sample.

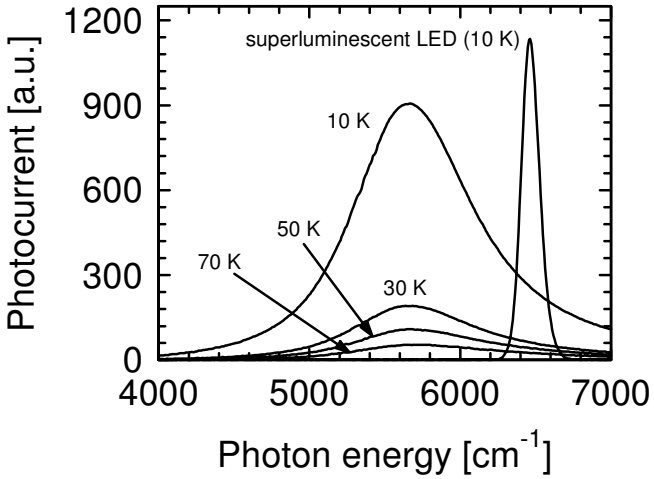

Fig. 2 - Photocurrent vs. photon energy curves for temperatures of 10, 30, 50, and 70 K. The peaked signal at 1.55 µm was obtained using an external SLED (P = 1 mW) as excitation source.

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Complementary characterization of hot electrons in AlGaN/GaN and AlN/GaN channels for high-power applications

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Complementary characterization of biased nitride two-dimensional electron gas channels is reviewed. Microwave noise technique for estimation of hot-phonon lifetime is presented. Effect of hot-phonon lifetime on relaxation of hot-electron energy and density of confined electrons is discussed.

Introduction

Nitride two-dimensional electron gas (2DEG) channels support excellent high-power performance of field-effect transistors (FET) at microwave frequencies [1]. At a high bias—typical for high-power FETs—fast dissipation of excess energy is needed to keep electrons confined in the 2DEG channel where the electron mobility is high. Spontaneous emission of LO phonons by high-energy electrons would be fast enough [2] unless hot LO phonons were accumulated and caused a bottleneck for the energy dissipation [3–6]. Hot phonons reduce the drift velocity [5, 6] and the field for the onset of confined–shared transfer [7]—a sort of real-space transfer (RST). As a result, the merits due to high mobility are lost already at moderate electric fields. The standard characterization—measurement of electron mobility and sheet density—does not provide with sufficient data for considering hot-phonon effects. The microwave noise technique suits for complementary characterisation of 2DEG channels subjected to the electric field applied in the plane of electron confinement [8–11]. The technique has been used to study hot electrons [10–13] and hot phonons [3, 8, 9, 14, 15] in AlGaN/GaN, AlN/GaN, and AlGaN/AlN/GaN channels. The usual technique for LO-phonon lifetime measurement is based on anti-Stokes line intensity decay in time-resolved Raman light scattering experiments [16]. However, this technique has not been applied to LO-phonon lifetime measurement in a nitride 2DEG channel designed for a high-power FET. The microwave noise technique for LO-phonon lifetime measurement [8] will be presented.

LO-phonon lifetime

The lifetime τ_{ph} of non-equilibrium LO phonons in respect to their disintegration into other phonon modes is defined as follows [8]:

$$\tau_{ph} = \hbar\omega\,[\,f_{ph} - (\,f_{ph})_{eq}]/(UI/N) \qquad (1)$$

where occupancy f_{ph} of the involved LO-phonon states is available from the power balance

$$UI/N = \hbar\omega/\tau_{sp}[(1+ f_{ph})\exp(-\hbar\omega/k_B T_e) - f_{ph}]. \qquad (2)$$

Here the supplied electric power UI/N is balanced with the power the electrons dissipate through spontaneous and stimulated emission of LO phonons and LO-phonon absorption, U is the voltage, I is the current, N is electron number in the channel, $\hbar\omega$ is the LO-phonon energy and τ_{sp} is the time constant for spontaneous emission ($\hbar\omega$ = 0.092 eV and $\tau_{sp} \approx$ 10 fs in GaN). The required electron temperature T_e is obtained from the noise temperature T_n measured in the field range where $T_n \approx T_e$ [13]. The noise is measured for two-electrode samples in the standard way [10–12]. Figure 1 illustrates experimental results for AlGaN/GaN. The RST

(confined–shared transfer) noise [7] manifests itself as a steep increase at E > 6 kV/cm at 293 K (Fig. 1, open circles, see also a similar increase at 80 K). In the field range where RST noise is weak, the noise temperature T_n approximately equals the hot-electron temperature T_e [11–13]. The noise temperature T_n as a function of the supplied power UI/N is illustrated in Fig. 2. The results on τ_{ph} are shown in Fig. 3.

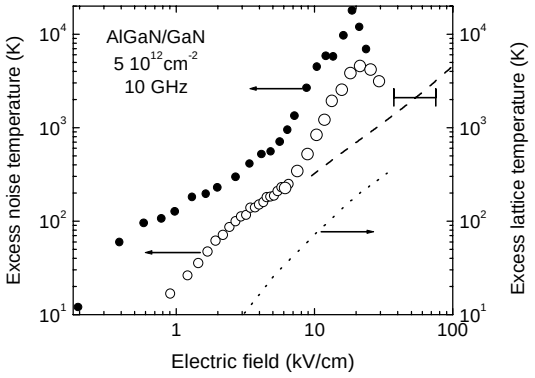

Fig. 1. Field-dependent excess noise temperature at ambient temperature [9]: 293 K (open circles), 80 K (closed circles). Hot-electron excess temperature at 293 K: luminescence data (H) [17], and $\tau_\varepsilon(E)$ data (dashes) [15]. Self-heating (dots) [8].

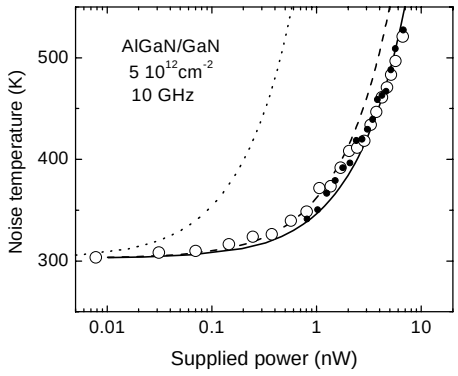

Fig. 2. Dependence of noise temperature on supplied power at room temperature for two samples: (open circles) [15] and (closed circles) [12]. Lines stand for empiric relation (3) where τ_{ph} equals: 250 fs (solid line), 350 fs (dashed line), and 3 ps (dotted line).

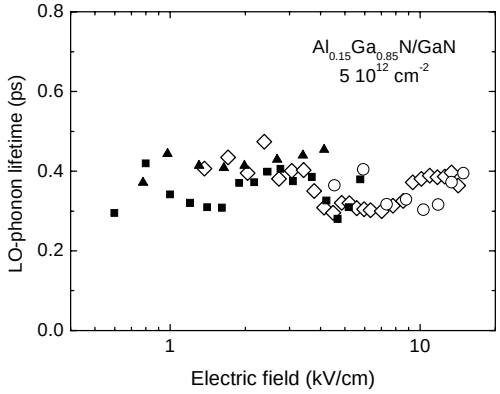

Fig. 3. LO-phonon lifetime for AlGaN/GaN 2DEG channel at different electric field and ambient temperature: 80 K—squares [8] and triangles [9], 303 K—diamonds [15], 373 K—circles [18].

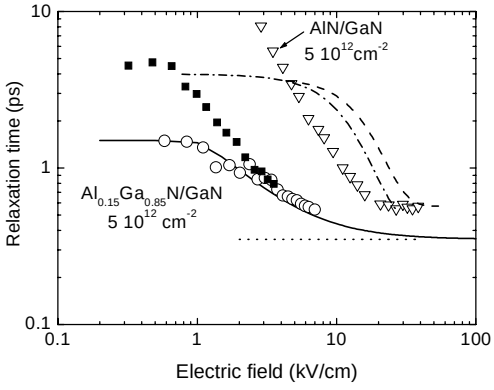

Fig. 4. Field-dependent electron energy relaxation time: AlGaN/GaN at 303 K (circles) [15], at 80 K (squares) [13]; AlN/GaN at 80 K (triangles) [3]. Relaxation time for confined–shared transfer in AlGaN/GaN: 303 K (dash) [15], 80 K (dash–dot) [9].

The experimental data of Fig. 2 obey the relation [14]:

$$UI/N = \Delta\varepsilon/\tau_{ph}\ \{\exp(-\Delta\varepsilon/k_BT_n)+ [\ \exp(-\Delta\varepsilon/k_BT_n)-1] /[\ \exp(\Delta\varepsilon/k_BT_L)-1]\}. \qquad (3)$$

At a low lattice temperature, $T_L << \Delta\varepsilon/k_B$, Eq. (3) reduces to Arrhenius plot: $UI/N = \Delta\varepsilon/\tau_{ph} \exp(-\Delta\varepsilon/k_BT_n)$. Thus, an estimation of the activation energy $\Delta\varepsilon$ and the time constant τ_{ph} is possible even if the values for $\hbar\omega$ and τ_{sp} are not known. Lines in Fig. 2 show, that $\Delta\varepsilon \approx$ 0.092 eV is close to the LO-phonon energy in GaN. The fitted time constant τ_{ph} is comparable with the mean values presented in Fig. 3. The LO-phonon lifetime $\tau_{ph} \approx 3$ ps—measured for GaN by Raman light scattering technique [16]—is too long for interpretation of the noise data in terms of Eq. (3) (Fig. 2, dotted line and circles).

Electron temperature and energy relaxation at high electric fields

The microwave noise technique is applicable for investigation of energy dissipation in the range of electric fields where the RST noise is insignificant. The RST noise is eliminated by substituting AlN for AlGaN. Under assumption that $T_n \approx T_e$ the noise experiments on AlN/GaN layers carried out over a wide range of bias [3] allow one to estimate the hot-electron energy relaxation time according to:

$$\tau_\varepsilon = k_B(T_e - T_L) / (UI/N) \quad (4)$$

where T_L is the lattice temperature—the temperature of all phonons except for those involved in the electron–LO-phonon interaction. Figure 4 illustrates $\tau_\varepsilon(E)$-dependence (triangles) for AlN/GaN. The energy relaxation time decreases as the field increases, but the decrease stops at the value near 0.55 ps (Fig. 4, triangles). Similar values of 0.5~ps have been obtained for GaN bulk samples during femtosecond optical pump and probe experiments [19, 20].

In AlGaN/GaN no significant dependence of the LO-phonon lifetime on electric field and lattice temperature has been found (Fig. 3), and an extrapolation of the mean value into the range of high electric fields has been suggested [15] (Fig. 4, dots). The extrapolated LO-phonon lifetime in AlGaN/GaN (Fig. 4, dots) is comparable with the measured high-field value of the electron energy relaxation time in AlN/GaN (Fig. 4, triangles) [3].

Let us exploit the idea that the hot-phonon lifetime sets the lowest limit for the hot-electron energy relaxation time at high electric fields [9, 15]. Solid line in Fig. 4 presents a possible extrapolation of the experimental data on hot-electron energy relaxation time (open circles) [15]. The extrapolated $\tau_\varepsilon(E)$ values (Fig. 4, solid line) are placed back into Eq. (4) in order to obtain the dependence of the electron temperature on electric field, $T_e(E)$, for AlGaN/GaN (Fig. 1, dashed line) [15]. The estimated electron temperature is in a reasonable agreement with the temperature T_e obtained from the hot-electron luminescence spectrum measured from the gate–drain region of a biased AlGaN/GaN transistor channel (Fig. 1, H)[17].

Confined–shared transfer

The extrapolated dependence of electron temperature on electric field $T_e(E)$ for AlGaN/GaN can be used for considering electron redistribution among subbands. Since the wave function penetrate into AlGaN layer when the electron is in the high-energy subband, the adjacent GaN and AlGaN layers share the high-energy electrons. The subband model [5] provides with the shared electron density as a function of the electron temperature, $n_{sh}(T_e)$ [7]. The dependence $n_{sh}(T_e)$ [7] together with the $T_e(E)$ dependence (Fig. 1, dashes), provides with the dependence of the shared electrons on electric field, $n_{sh}(E)$.

Within a two-level model, the product of the shared and the confined electron densities $n_{sh}n_{cf}$ is the measure of spectral intensity of the occupancy fluctuations. The product has the maximum in the field range where the spectral intensity of current fluctuations has the maximum too [7, 9, 15]. The ratio n_{sh}/n_{cf} enters the expression for the relaxation time of the occupancy fluctuations [9, 15]. The fitted dependence of the relaxation time on electric field is illustrated in Fig. 4. The high-field value is close to the mean value of LO-phonon lifetime.

The effect of hot phonons is two-fold: (i) the hot-phonon lifetime is used to extrapolate the electron temperature into the range where the confined–shared transitions manifest themselves, and (ii) the high-field value for the relaxation time of the confined–shared transitions seems to be limited by the hot-phonon lifetime.

Conclusion

Microwave noise technique has been used for estimation of the lifetime of non-equilibrium LO phonons in nitride 2DEG channels. The LO-phonon lifetime is the central parameter that decides hot-electron energy dissipation and real-space transfer at high electric fields.

Acknowledgements

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1/f Noise Measurement and Theory in GaN HFETs, other Devices and Systems

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We report investigation of 1/f noise through measurement of heterostructure field effect transistors (HFETs) grown on various substrates, SiC (lowest channel noise), Sapphire, and HVPE. Our experimental results are compared to quantum 1/f theory α_{theor}. New formulas for piezo-1/f noise in GaN, phase noise, irradiation, and spin flip are given.

1/f noise is given as resistance fluctuations δR/R. The quantum 1/f spectral density is

$$fR_{DS}^{-2} < (\delta R_{DS})^2 >_f = (I_{Ch}/V_{DS}^2)\int_0^{V_{sat}} \frac{\alpha_{coh} dV}{q\mu N'^2} + \int_{V_{sat}}^{V_{DS}} \frac{\alpha_{conv} q v_s^2 dV}{V_{DS}^2 q\mu I_{Ch}} = \frac{1}{V_{DS}\mu}\{\frac{\alpha_H^{coh} I_{ch}}{qZ^2 D_{eff}^2 V_{th} V_{DS}} + \frac{\alpha_H^{conv} q v_s^2}{I_{ch}}(1 - \frac{V_G^*}{V_{DS}} + \frac{V_{th}}{V_{DS}})\}. \quad (1)$$

Here $\alpha^{coh}=2\alpha/\pi=4.6\ 10^{-3}$, $\alpha^{conv}=4\alpha/3\pi)<(\Delta \mathbf{v}/c)^2>$, $\alpha=1/137$. The main experimental results are:

(1). At Vg = 0, the lowest $S_{\delta R/R}(f)$ was measured for a HFET on the SiC substrate with $S_{\delta R/R}(f) = 3.9\cdot10^{-13}$, followed by with $S_{\delta R/R}(f) = 2.0\cdot10^{-11}$ on Sapphire, and the noisiest, with $S_{\delta R/R}(f) = 7.8\cdot10^{-11}$ on HVPE. Inclusion of the source resistance noise improves theory agreement.

(2). When Vg changes from 0 volt to –3.0 volts for HEFT on SiC, the $S_{\delta R/R}(f)$ increases from $1.24\cdot10^{-12}$ to $1.64\cdot10^{-10}$, about two orders of magnitude. Our results are shown in Table 1.

The apparatus is shown in Fig. 1 below, a typical spectrum and background in Fig. 2.

Table 1: 1/f Noise Coefficients α Measured in GaN HFET Devices

Substrate	Device	R_{DS}/Ω	V_{DS}/V	$fS_{\delta R/R}$	α_{exp}	α_{theor}
HVPE						
	STD3	36	0.9	7.8E-11	9.99E-5	3.0E-5
Sapphire						
	STD7	20.5	0.27	2.0E-11	2.06E-5	2.7E-5
SiC						
	STD12	37.3	0.53	3.9E-13	2.69E-7	1.5E-7
	STD4	40.4	2.1	1.24E-12	7.92E-7	3.3E-6

This is electrodynamic Q1/f noise. More details, if/when interest in 1/f+phase noise develops.

For piezoelectric Q1/f noise in larger, spontaneously polarized, GaN samples, we obtain

$$\alpha_H = fNS_{\delta j/j}(f) = [1/(1+s')](4g/3\pi)(\Delta \mathbf{k}/k_s)^2 + [s'/(1+s')]\{2g/\pi[1-(<\mathbf{k}>/k_s)^2]\}, \quad (2)$$

where v_s is the speed of sound, $<\mathbf{k}>=m^*<\mathbf{v}>/\hbar$, $|<\mathbf{v}>| = u$ is the drift velocity of the carriers, and

$$k_s = m^* v_s/\hbar; \quad s' = (gN'\hbar/\pi m^* v_s)(v_s/u)^3 F(u/v_s). \quad (3)$$

N' is the number of carriers per unit length of the sample in the direction of current flow, and

$$F(u/v_s) = 2(u/v_s)\{1 + 1/[1 - (u/v_s)^2]\} + \ln[1-(u/v_s)]^2 - \ln[1+(u/v_s)]^2. \quad (4)$$

The coherence parameter s' is the ratio of the coherent piezoelectric energy of the drift motion divided by the additional kinetic energy of the carriers introduced by the drift velocity u.

The phase noise $L(f_m)$ of oscillators is described by the empirical Leeson formula, with a second term that was introduced by the author based on the quantum 1/f theory:

$$L(f_m) = 10\log\{\frac{1}{2}((\frac{f_0}{2Q_l f_m})^2 + 1)(\frac{f_c}{f_m} + 1)(\frac{FkT}{P_s}) + \frac{f_0^2}{2 f_m^2}\frac{1}{4Q_l^4} S_{\delta\gamma/\gamma}\} \quad (5)$$

Here Q_l is the loaded quality factor, f_0 is the resonance frequency, f_c is the flicker corner frequency without Q1/f effect in dissipation, and $S_{\delta\gamma/\gamma}$ is the spectral density of fractional fluctuations

in the dissipation rate γ that causes the free oscillations of the resonator to attenuate. P_s is the amplifier's input signal power, and F is its noise figure. The bracket [ ] in Eq. (5) is $S_\phi/2$.

Quantum 1/f theory gives the ratio between the 1/f noise power after and before irradiation dose J

$$R = S'/S = [(\mu_l-\mu)^2S_d+\mu^2S_l]/\ [(\mu_l-\mu_o)^2S_d+\mu_o^2S_l] \quad \text{for FET/HFET} \quad (6)$$

$$R \approx (1/\tau_o +\sigma\nu\kappa J) \quad \text{For junction devices (pn, BJT, HBT)} \quad (7)$$

For spin polarized currents j in magnetic compound semiconductors, we obtain the basic formula

$$S_{\delta j/j} = \Gamma^{-2}S_\Gamma(f) = 32\alpha\mu^4H^2N^2/3\pi fe^2c^2\hbar^2. \quad (8)$$

This is the spectral density of fractional quantum 1/f fluctuations in the rate Γ of spin-flip or decoherence (electrodynamical Q1/fEff. only). This spectral density of fractional fluctuations will affect the spin-polarized leakage current j through the device. There is also shot noise $S_{\delta j/j}=2ej$.

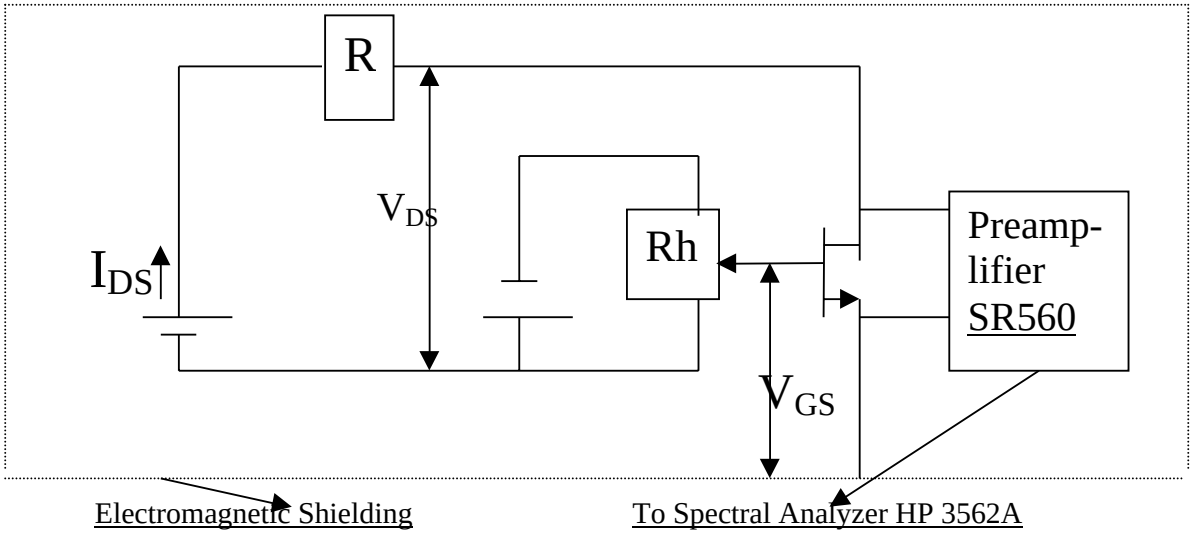

Fig. 1: Experimental Set-Up. As shown in Fig. 1, the gate voltage V_G is controlled with a Rheostat Rh.

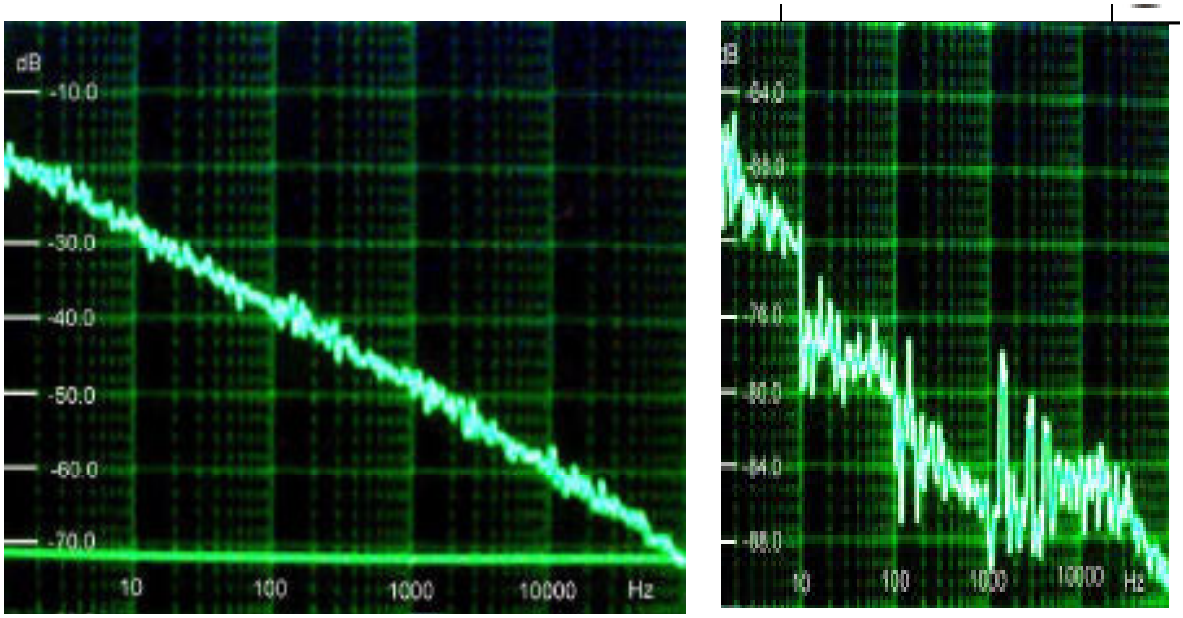

Fig. 2: Typical 1/f noise spectrum of the HFET channel, with much lower background on the right.

The study of low-frequency noise peculiarities in HEMT structures under self-heating conditions

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The features observed in the carrier transport and noise spectra in two-dimensional AlGaN/GaN conducting channels are explained within a model based on overheating effects, dynamic redistribution of potential as well as hopping transport of carriers in the barrier.

The group III-nitride based devices aimed to use in high power and high temperature microelectronic applications operate at increased specific dissipated power. As the electric power and the operation temperature will be increased, the role of thermal budget become to be more critical. Under these conditions investigation of transport and noise properties should be carried out with taking into account both hot electrons and self-heating effects due to dissipated Joule electric power. If real temperature of the conducting channel of a device is known, the contributions of electric field and temperature effects can be separated. Such a separation is important to clarify the thermal budget of devices and optimize the device performance.

In this report we present the results of investigation of low-frequency noise spectra in group III-nitride based AlGaN/GaN gateless (transmission line model patterns of different length and of the same channel width) heterostructures grown on sapphire. We study also the current – electric field, I-E, characteristics. The obtained I-E characteristics (Fig.1) are strongly nonlinear although the considered field range is still below the fields of well-developed hot-electron regime expected from theoretical predictions [1, 2].

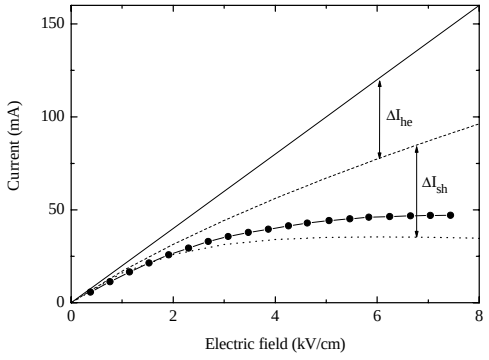

Fig. 1. The result of calculation I vs E for the device with channel length of 25 μm and width of 100 μm. Solid line is ohmic I-E curve, arrows show current decrease due to hot-electron (ΔI_{he}) and self-heating (ΔI_{sh}). Circles are experimental data measured at 300 K.

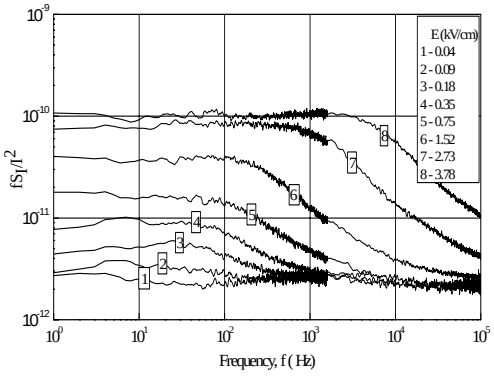

Fig. 2. Spectra of the normalized current noise for different values of the electric field E measured at T=300 K for the device with the channel length of 25 μm and the width of 100 μm.

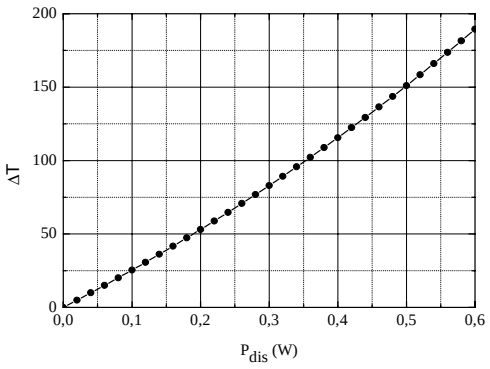

Fig.3. Dependence of the temperature rise on the dissipative power in the channel of 25 μm length. T_0=300K.

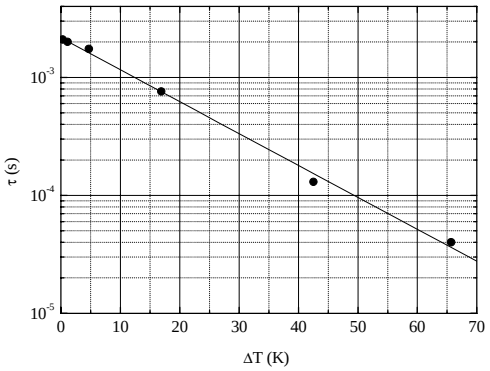

Fig.4. Dependence of the characteristic time parameter on the channel overheating. T_0=300K.

The noise spectra also reveal considerable deviation from 1/f law predicted in the McWhorter (fluctuations of concentration) [3] or Hooge (mobility fluctuations) [4] models. The main feature of noise spectra is an increase of the 1/f noise level in the low-frequency range of measured spectra with increasing the applied voltage as shown in Fig.2. Between the low-frequency and high-frequency 1/f spectral ranges a transition region appears which is characterized by strong deviation from the 1/f behavior. Both the noise level in the low-frequency range and the characteristic frequency of the transition region depend considerably on the applied voltage.

Analysis of the high-frequency interval of the noise spectra measured for devices with different channel lengths shows the normalized current noise spectral density to be inversely proportional to the channel length that is typical for the Hooge noise. Remarkably that in this frequency interval the normalized noise level is independent of the applied voltage. It should be considered that the observed features are caused by heat dissipation. In view of the fact that the self-heating is present, the analysis of the noise spectra in both low-frequency and transition intervals demands separation of temperature and field effects. To this end, we formulate a theoretical model based on (i) heat dissipation and heat-transfer modeling in the device and (ii) self-consistent solution of coupled nonlinear equations for the channel current I and the channel temperature rise ΔT [5]. The results of simulation are presented in Fig.1 and Fig.3 where the temperature rise ΔT versus dissipated power P_{dis} is depicted. The latter result allows us to plot the time parameter τ, that corresponds to frequency separating low-frequency 1/f range and transition one, as function of ΔT. An exponential dependence of τ is clearly seen from Fig.4 that reflects the activation process like hopping conductivity which can occur in the barrier layer. In the latter case the electrons in the barrier layer transferred by hops contribute to a slow component of the noise.

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Gate Leakage and Current Collapse in AlGaN/GaN HFETs and Their Removal by a Novel Insulated Gate Structure Using Al_2O_3

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Mechanisms of gate leakage and current collapse in AlGaN/GaN HFETs are clarified through detailed electrical measurements. A novel Al_2O_3 insulated gate structure is proposed to remove them.

Introduction

The AlGaN/GaN heterostructure field-effect transistor (HFET) has become a key high-frequency power device. However, conventional Schottky-gate (SG) HFETs suffer from large gate leakage and drain current collapse. In this paper, attempts were made to clarify their mechanisms through detailed electrical measurements, and to remove them by a novel Al_2O_3 insulated gate (IG) structure.

Mechanism of Gate Leakage and Drain Current Collapse

As shown in **Fig.1**, detailed electrical properties of the ungated portion and Schottky–gated portion of the device were investigated separately. The gateless HFET device was subjected to plasma treatments and surface passivation processes, including our novel Al_2O_3–based surface passivation[1)]. DC ***I–V*** curves of gateless HFETs were highly non-linear due to virtual- gating by surface states. Pulse response of the gateless HFETs is schematically shown in **Fig.2 (a)**. After drain stress, recovery transients of air-exposed, H_2 plasma-treated and SiO_2–deposited gateless HFETs had an initial large-amplitude exponential transient followed by a smaller, slow and highly non-exponential response. The former was emission from deep donors at E_c–0.37 eV as shown in **Fig.2(b)**. The latter was that from surface states. Capture transients with stress-dependent capture barriers were also observed during stress. XPS study indicated that 0.37 eV donors are N-vacancy related. N_2-plasma treated and Al_2O_3-passivated samples showed square responses without capture/emission transients.

Temperature dependences of Schottky *I–V* curves were extremely small and reverse currents were anomalously large. They were explained by the "thin surface barrier" (TSB) model[2,3)] where thermionic field emission and field emission through the TSB region formed by deep donors produce leakage current paths. Comparison of ideality factor between theory and experiment is shown in **Fig.3**.

By combining the results on gateless HFETs and Schottky diodes, a new unified model of near-surface electronic states for the free surface and Schottky interface of AlGaN, shown in **Fig.4 (a),** is proposed. It consists of a U-shaped surface state continuum and N-vacancy related near-surface discrete deep donors. The model can explain the observed large gate leakage. Explanation of drain current collapse under drain stress and gate stress is sown in **Fig. 4 (b) and (c)**, respectively.

AlGaN/GaN HFETs with a Novel Al_2O_3 Insulated Gate Structure

To remove gate leakage and current collapse, HFETs having an Al_2O_3 insulated gate (IG) structure shown in **Fig.5(a)** were fabricated and tested. Al_2O_3 was formed ECR O_2 plasma oxidation of molecular beam deposited Al film. According to XPS analysis, Al_2O_3 layer had a large bandgap of 7.0 eV and a large conduction band offset of 2.1 eV with respect to AlGaN, as shown in **Fig. 5(b)**, leading to reduction of leakage currents by many orders of magnitude as compared with Ni-Schottky gate (SG) and SiN_x-IG structures. I-V characteristics of the novel Al_2O_3 IG-HFET, shown in **Fig.6(a)**, gave a maximum g_m of 120 mS/mm. The measured percentage collapse values of drain currents after applying a gate stress of V_{GS} = -8V for 10 s are shown in **Fig. 6(b).** No current collapse was observed in the Al_2O_3 IG-HFETs, whereas SG-HFETs showed pronounced collapse.

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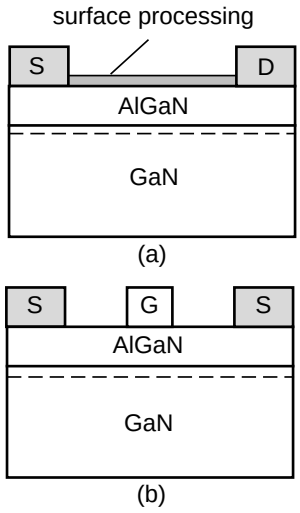

Fig.1: Sample structures.

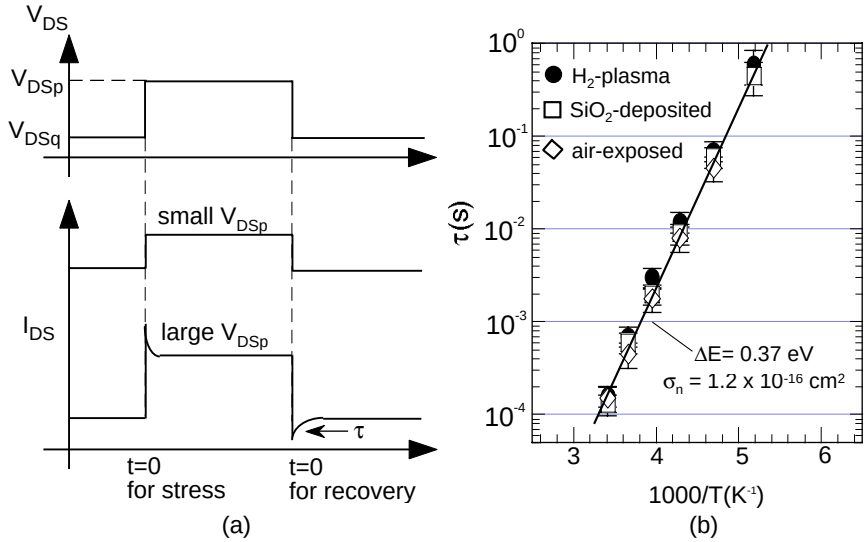

Fig.2: (a) Pulse waveforms of gateless HFET and (b) Arrhenius plots of τ for emission.

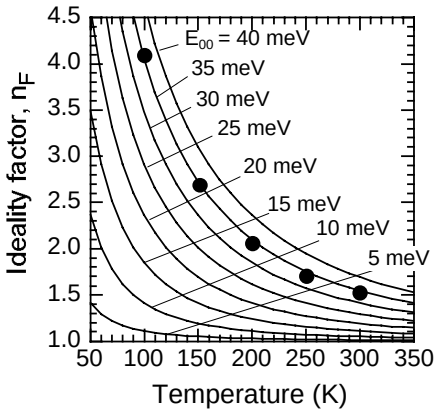

Fig.3: Comparison of ideality factor.

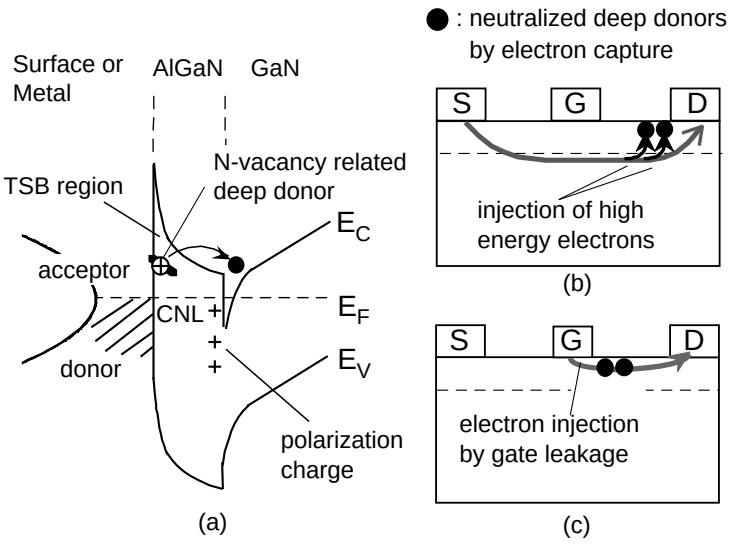

Fig.4: New models for state distribution, (b) collapse under drain stress and (c) collapse under gate stress.

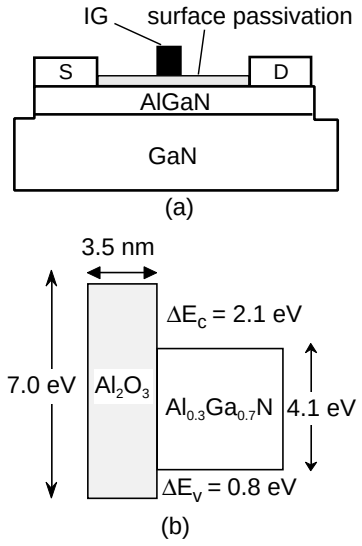

Fig.5: Al_2O_3 IG-HFET.

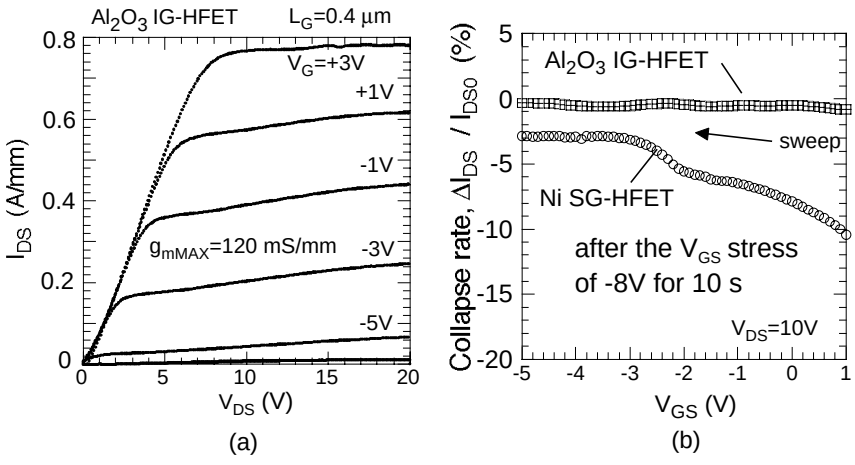

Fig.6: (a) Drain I-V characteristics and (b) percentage collapse values.

Current Collapse in AlGaN/GaN HEMT's analyzed by means of 2D device simulation

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In this work, we analyze *for the first time,* by means of 2D numerical device simulations, the influence of surface states on the DC and pulsed characteristics of AlGaN/GaN HEMT's, and we show that the concomitant presence, at the ungated surface, of polarization induced negative charge and surface hole traps can explain, *without invoking any other hypothesis*, all dispersive effects in AlGaN/GaN HEMT's and, in particular, both gate- and drain-lag experiments. In the presence of polarization charge densities of the order of 10^{13} cm^{-2}, bands are upward bent at the ungated surface and consequently the dynamics of surface states is governed by hole exchange with the valence band.

Drain-current (I_D) collapse is the major factor limiting the output-power density at microwave frequencies in GaN-based FET's [1]. Its detrimental consequences on device performance have been put into evidence by using different experimental techniques, including measurements of pulsed drain current (I_D) vs drain-source voltage (V_{DS}) characteristics, gate- and drain-lag transients, transconductance (g_m) frequency dispersion, rf response [1,2,3]. Several studies suggest that surface defects can play a predominant role in originating the observed device behavior. Indications in favour of surface-induced I_D collapse are the following: dispersion effects are reduced by SiN surface passivation which decreases the density of deep levels [4]; in unpassivated devices dispersion is suppressed by dipping the sample in isopropanol [5] and restored when isopropanol is removed; p^+ or n^+ layers on access regions remove dispersion [5].

Devices used in this work are unpassivated $Al_{0.35}Ga_{0.65}N$/GaN HEMT's grown by MOCVD on SiC substrates. The gate length is 0.7 μm, whereas gate-source and gate-drain spacings are 0.7 μm and 2 μm, respectively [5]. I_D-V_{DS} characteristics measured in DC conditions and pulsing either V_{GS} or V_{DS} are shown in Figs. 1 and 2. In agreement with previous literature [2,6], a significant I_D collapse is evident in the V_{GS} turn-on pulsing mode in Fig. 1, whereas a small increase in I_D (with respect to DC conditions) is observed when V_{DS} is pulsed, see Fig. 2. The I_D collapse in the V_{GS} pulsing mode explains the rf large-signal I_D collapse and the attendant power degradation typically observed in GaN FET's. Experimental $I_D(t)$ waveforms are reported in Figs. 3 and 4 for the V_{GS}- and V_{DS}-pulsing mode, respectively. As can be seen, slow transients affect the $I_D(t)$ response in both cases. Consistently with the pulsed I_D-V_{DS} curves shown in Figs. 1 and 2, I_D increases with time in Fig. 3 (pulsed I_D smaller than the DC I_D, see Fig. 1, while it decreases with time in Fig. 4 (pulsed I_D greater than the DC I_D, see Fig. 2. The observed pulsed behavior reflects into the $g_m(f)$ curves of Fig. 5, showing a downward dispersion at around 1kHz.

2D drift-diffusion simulations of the HEMT under study were carried out using the code DESSIS (ISE A.G.). Positive and negative polarization charges with a density of $1x10^{13}$ cm^{-2} were placed at the AlGaN/GaN hetero-interface and at the ungated AlGaN surface, respectively. Surface-state traps were also placed at the ungated AlGaN surface. We assumed donor-like traps with energetic position E_t= E_V+0.4 eV, electron and hole capture cross sections $\sigma_n=\sigma_p=1x10^{-15}$ cm^2, density $N_{SS}=5x10^{12}$ cm^{-2}. Due to the strong negative polarization charge density, bands are locally bent upwards, so that the ungated surface is populated with holes in the concentration of 10^9-10^{13} cm^{-3} (depending on the bias conditions). Moreover, only surface states relatively close to the top of the valence band can effectively be modulated by changes in the applied voltages and the ensuing transients are therefore governed by hole emission/capture from/into these states. Simulated DC and pulsed I_D-V_{DS} characteristics at V_{GS}=0 V are shown in Fig. 6, whereas simulated $I_D(t)$ transient waveforms are reported in Figs. 7 and 8 for the V_{GS} and V_{DS} turn-on pulsing mode, respectively. As can be seen, simulations are able to reproduce all of the relevant features characterizing the corresponding experimental curves shown in Figs. 1-4. The underlying physics, for the different pulsing modes, will be explained during the presentation.

In conclusions, a physics-based model of transient and collapse phenomena in GaN-based HEMTs has been presented, which demonstrates that the presence of surface hole traps, together with polarization-induced negative charge, can consistently explain all dispersive effects observed in the various experimental conditions.

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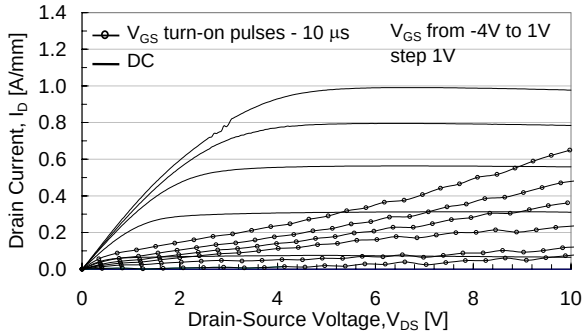

Fig. 1. Experimental I_D-V_{DS} characteristics obtained in DC and by pulsing V_{GS} from –4V to the quoted V_{GS} (10-μs pulse width, 0.01% duty cycle).

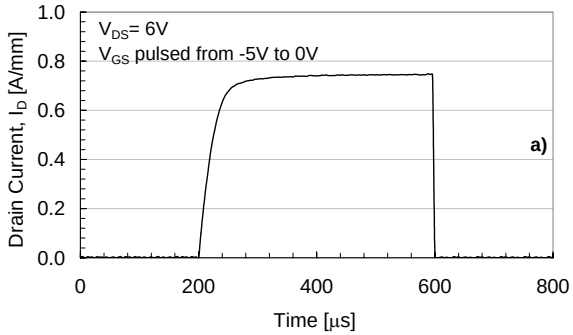

Fig. 3. a) Experimental I_D(t) transient in response of a V_{GS} turn-on pulse at V_{DS}= 6V.

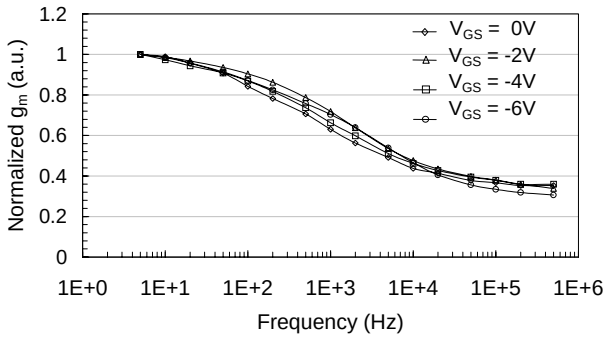

Fig. 5. Experimental g_m(f) low-frequency dispersion curves.

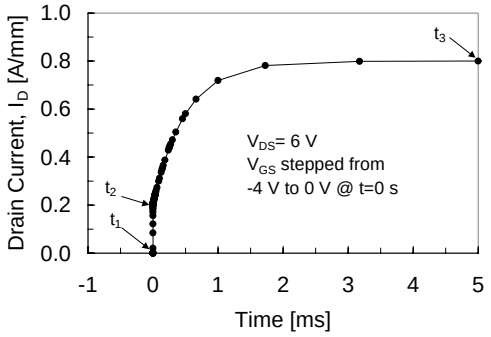

Fig. 7. Simulated I_D(t) transient following a V_{GS} turn-on step.

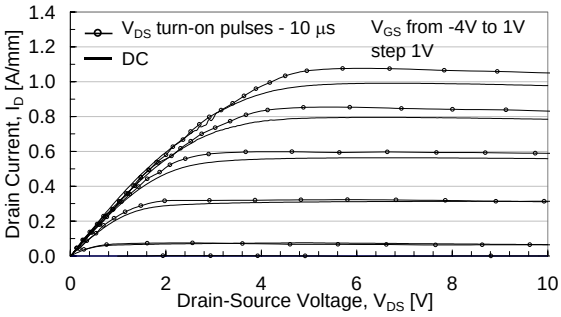

Fig. 2. Experimental I_D-V_{DS} characteristics obtained in DC and by pulsing V_{DS} from 0 V to the x-axis value (10-μs pulse width, 0.01% duty cycle).

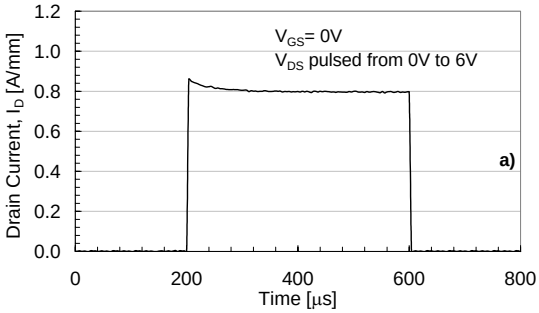

Fig. 4. a) Experimental I_D(t) transient in response of a V_{DS} turn-on pulse at V_{GS}= 0 V.

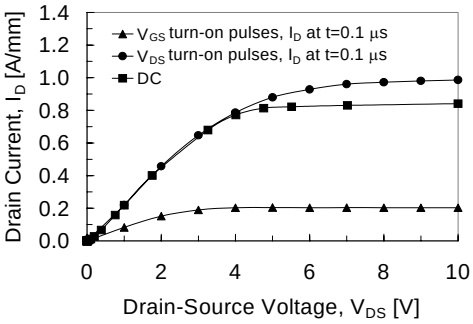

Fig. 6. Simulated I_D-V_{DS} characteristics obtained in DC and by pulsing either V_{GS} (from –5 V to the quoted V_{GS}) or V_{DS} (from 0 to the x-axis value).

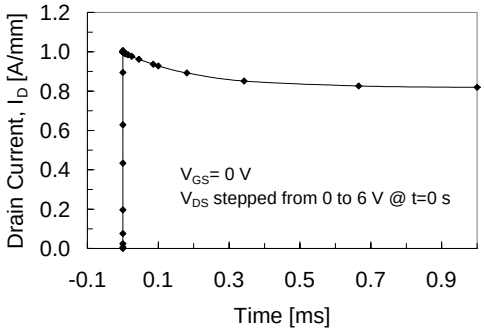

Fig. 8. Simulated I_D(t) transient following a V_{DS} turn-on step.

Study of physical and technological limits for AlGaN/GaN transistors

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In this work we studied main concepts of AlGaNGaN transistor development which includes 3D simulation of pulsed power dissipation and consideration of transistor processing with accent on 100 nm T-shaped gate fabrication, Ohmic contact formation, and passivation. All considerations are followed by device characterization. Limits of power generation for III-nitrides are determined from BN transistor simulation which has ultimate properties among III-V materials.

3D thermal simulation Due to outstanding optical, thermal, and electron transport properties of III-nitrides they are very actively studied with the main aim of applications as materials for LEDs and high-power microwave transistors. These devices produce large amount of heat over a small area, which could result in deterioration of the performance of the devices to their destruction. An efficient heat sinking is especially necessary when heat dissipates in nano-regions like in 2DEG under 50-300 nm gate of power transistor. Therefore, 3D thermal simulation is required with paying attention to creation as concise as possible model for the devices.
In this study, we carried out 3D simulation of pulsed thermal dissipation in typical AlGaN/GaN HEMTs on different technologically important substrates (SiC, AlN, and Si) with transistor chip area 1×1 mm^2. Due to ultimate thermal and electronic properties of BN among all III-V materials, BN transistor was studied to show physical limits for applications of III-nitrides. Investigated semiconductor structures are presented in Table. The heat source in transistors is at the boundary between undergate and buffer layers (at a depth d_c=20 nm) and its geometric sizes are the same as those of the gate. The gate consists of 15 parallel fingers (0.3×700 μm^2) 52 μm apart from each other with total gatewidth of 10.5 mm. For cooling of the semiconductor structures, $10 \times 10 \times 1$ mm^3 copper heatspreader (the backside is at T_0=300 K) is used. The time diagram (Fig. 1) consists of periodically repeated bunches with 88 pulses (100 W or $\sim$10 W/mm and 0.5 μs duration) in each bunch. Nonstationary temperature distribution was determined from nonlinear heat equation using algorithms developed in [1]. Fig. 2 shows spatial maximum temperature distribution (structure 2) at the boundary between undergate and buffer layers after first bunch of pulses. In 3 bunches, heat dissipated in all structures becomes equal to heat sinking through heatspreader bottom. For 100 W pulses, the maximum temperature rise (SiC) does not exceed 100 K (5 K higher for AlN and 28 K for Si substrates). The temperature rise for structures with $Al_{0.3}Ga_{0.7}N$ (20 nm) undergate layer with lower thermal conductivity compared to GaN(20 nm) is 11 K higher. For 100 K rise, the maximum dissipated power of more than 30 W/mm could be achievable in case of BN transistor, which arranges the limit of power dissipation for III-V materials. Investigation of BN growth, doping, and device processing [2] is necessary for future progress of microwave devices.

No	Undergate layer (d_c=20 nm)	Buffer (d_b=1 μm)	Nucleation layer (d_p=20 nm)	Substrate (d_w=300 μm)	T_{max}^{max}, K (T_0=300 K)
1	GaN	GaN	AlN	SiC	389
2	$Al_{0.3}Ga_{0.7}N$	GaN	AlN	SiC	400
3	$Al_{0.3}Ga_{0.7}N$	GaN	—	AlN	405
4	$Al_{0.3}Ga_{0.7}N$	GaN	AlN	Si	428
5	BN	BN	AlN	SiC	331

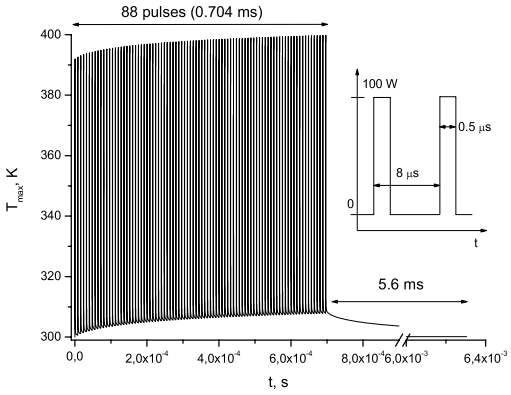

Figure 1: Time evolution of maximum temperature T_{max} during first bunch for structure No 2.

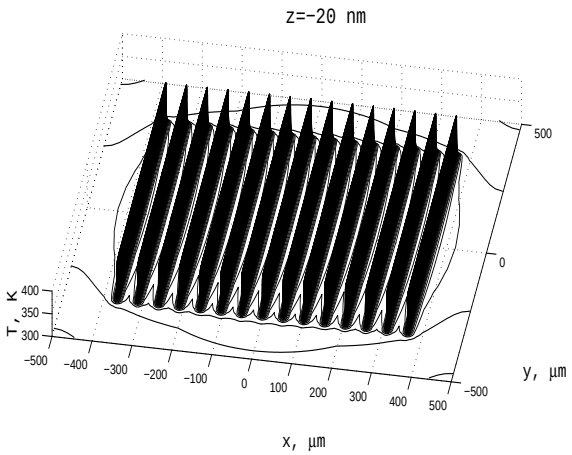

Figure 2: Maximum temperature distribution in channel after 88^{th} pulse of the first bunch (structure No 2).

Processing: Ohmic contacts, sub-100 nm T-gate, and passivation Results of the Ohmic contact formation and optimization for different metal schemes (fig.3) will be presented [3] for MOCVD AlGaN/GaN structures on sapphire substrates (L. Eastman, Cornell University). Ta/Al/Ni/Au metal combination showed the lowest contact resistance of only 17% from the total source-drain resistance. 100 nm T-shaped gate fabrication [4] and Si_3N_4 passivation [5] will also be discussed. After passivation, ECR plasma etching was applied to form holes in Si_3N_4 for air bridge interconnections between sources. Then, substrates were thinned from backside to 50-80 μm and laser cut. After that devices were packaged. I-V characteristics of fabricated AlGaN/GaN transistors were not sensitive to illumination and free from hysteresis (Fig. 4). Transconductances in the range 60-100 mS/mm and breakdown voltages greater than 40 V were observed for devices with 0.3 μm gatelength. As a result, full processing of AlGaN/GaN transistors was developed (from mesa etching to device packaging).

References

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[3] V. L. Gurtovoi *et al*, *Abstracts of 2-nd Russian Conference "Gallium, Aluminum and Indium Nitrides"*, February 3-4, 2003, Saint Petersburg, p. 17.

[4] V. L. Gurtovoi *et al*, *Proc. of XXVI Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE-02)*, 21-25 May, 2002, p. 61.

[5] S. Yu. Shapoval *et al*, *Proc. of 10^{th} Int. Symp. Nanostructures: Physics and Technology*, June 17-21, 2002, p.101.

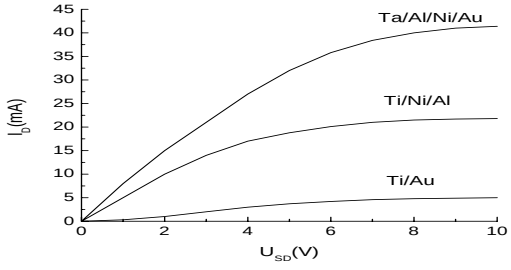

Figure 3: I-V characteristics of gateless structures with different Ohmic contacts.

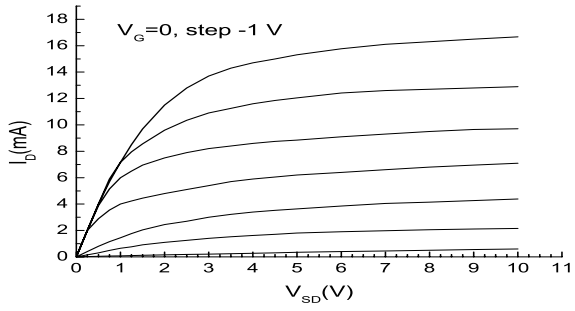

Figure 4: I-V characteristics of a 0.3×50 μm^2 AlGaN/GaN HEMT.

Performance limits of AlGaN/GaN HEMT's

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The impacts of loading, including self-heating, channel width, and the number of, and pitch between, channels on CW efficiency are presented for undoped, polarization-induced AlGaN/GaN HEMT's. The frequency response, and drain-source breakdown voltage, are also given as functions of gate length. Examples of the experimental class B CW power-added efficiency dependence on layout designs are included.

Introduction

Gallium Nitride has an electric field strength of ~ 3 MV/cm, with electron average transit velocity of ~ 1 x 10^7 cm/s. It is normal to use a thin, large bandgap barrier, such as $Al_XGa_{1-x}N$, to confine the electrons. There is a strong electrical polarization in the pseudomorphic undoped $Al_XGa_{1-x}N$ barrier grown on the Ga-face of GaN [1]. This induces a 2DEG of ~ 1 x 10^{13}/cm^2 in the GaN, which has a lower electrical polarization, near the heterojunction, when .30 < x < .35, and if the barrier is below the critical thickness for strain relaxation. The drain-source breakdown voltage depends directly on the gate length in HEMT's fabricated from this structure, being 80 V for a .25 μm gate. The extrinsic unity current-gain frequency depends on the reciprocal of the gate length, and is 50 GHz for a .25 μm gate, while the extrinsic unity power gain frequency for this HEMT is 100 GHz.

Design Parameters Limiting Performance

For the removal of heat, semi-insulating SiC is the best substrate for the AlGaN/GaN HEMT's[2]. For a HEMT designed for 10 GHz CW operation, channel widths of ~ 150 μm, separated by 50 μm is a good layout design. The temperature rise can be simulated in the channel, yielding $\Delta T = 13.5\ P_H + .2\ P_H^2$ where P_H is the normalized heat power dissipated, in W/mm. The channel portion of the source-drain resistance rises in proportion to $(T/T_o)^{1.8}$ where To is the heat sink temperature of ~ 300°K. The channel width is a key design parameter, since the signal voltage drops with distance from the drive point. Our experimental determination of this voltage drop, using a test structure with connections at both ends, and compared with operating transistors with two parallel gates 50 μm apart, has led to an efficiency factor dependent on gate width[3]. For our mushroom-shaped gates with 120Ω /mm DC resistance, it is:

$$\eta_W = \left[1 - .5\left(1 - \frac{1}{\cosh^2(\alpha W_g)}\right)\right] \qquad (1)$$

where W_g is the gate width, and α = 2.6/mm at 10 GHz. Another key parameter is the phase delay between channels in a manifold layout. This is determined by the number of channels on each side of the drive point, and the pitch separating the channels[3]. The efficiency factor to cover this parameter is:

$$\eta_\theta = \left[\sin\left(\frac{N\theta}{2}\right) \Big/ N\sin\left(\frac{\theta}{2}\right)\right]^2 \qquad (2)$$

where N is half the number of channels and θ is the phase shift, between the channels, of about 15° in this 10 GHz example. There is also a loading efficiency factor, which is:

$$\eta_L = R_L \Big/ \left[R_L + 2\,(R_S + R_D)\right] \qquad (3)$$

The overall efficiency is the product of these three factors times the theoretical limiting efficiency for the class of operation.

For layout with two, in-line gates, CW power levels of 11-12 W/mm at 10 GHz have been obtained. For ten parallel channels, each 150 μm wide, with 50 μm pitch, 6.7 W/mm has been obtained. Data on several HEMT's, each with 2 parallel gates, with a variety of gate widths are shown in chart I. In chart II, the data for several designs for 1.5 mm periphery are shown for comparison.

CHART I

CW class B operation at 10 GHz: experimental power-added efficiency dependence on channel width at 15 V_{ds} (low self-heating) with 50 μm separation between two channels.

Layout	Power-added efficiency	Load
2 x 100 μm	.687	(238 // j 312) Ω
2 x 150 μm	.680	(175 // j 257)Ω
2 x 200 μm	.655	(131 // j 233)Ω
2 x 250 μm	.630	(100 // j 179)Ω

CHART II

Class B CW, and pulsed, power-added efficiency for 1.5 m HEMT, with 50 μm pitch with different layouts for .3 μm gates, at 10 GHz.

Layout	CW η_{PA} (10 V_{ds})	CW η_{PA} (20 V_{ds})	Pulsed η_{PA} (35 V_{ds})
6 x 250 μm	.57	.54	.37
8 x 187.5 μm	.62	.62	.45
10x 150 μm*	.57	.58	.49
12 x 125 μm	.53	.55	.44
	Optimum load	28Ω load	40Ω load

*10 W CW at 40% η_{PA} at 30 V

Conclusion

AlGaN microwave power HEMT amplifier limits of efficiency for class B operation are presented and explained., based on experimental results. Small periphery devices yield 11-12 W/mm, at 40% power-added efficiency, while large periphery, manifold layout devices yield up to 6.7 W/mm with 40% power-added efficiency at 10 GHz.

References

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[3] V. Tilak, PhD thesis, Cornell University (2002)

Enhancing the Microwave Power Capabilities of AlGaN/GaN HEMTs

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Abstract

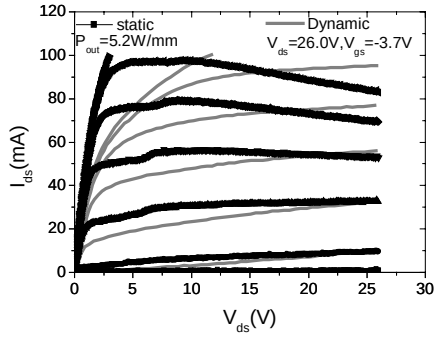
This paper details our work on gaining a better understanding of mechanisms leading to rf-power limitations of GaN/AlGaN high power transistors for microwave applications. Current slump effects e.g. the degradation of the usable I/V-output characteristics at high power microwave operation as compared to the static I/V-characteristics play the decisive role in power reduction. We performed a thorough investigation of this effect using dynamic I-V pulse analysis. A comparison of the dynamic I/V- versus the static I/V- characteristics of power cells from two different wafers (Fig. 1) showed significant differences in power reduction as a result of current collapse. The steady state working point of the dynamic (pulsed) measurements corresponded to the bias point of load-pull measurements on the same devices leading to a power density of 5.2 W/mm for wafer A and 3.9 W/mm for wafer B respectively. On the basis of special biasing conditions during pulse measurements, these trap related anomalies can be classified as gate lag and drain lag effects. For the steady state biasing conditions related to Fig. 1 the drain lag effect is considered to be the pronounced mechanism of current degradation indicating trap states in the buffer or the vicinity of the 2DEG.

In order to observe the gate lag effects, we compared the two characteristic curves measured under two different biasing conditions, one at V_{ds}=0.0V, V_{gs}=0.0V and other at V_{ds}=0.0V, V_{gs}=-7.0V as shown in Fig. 2. The pulsing from a steady state biasing point V_{ds}=0.0V, V_{gs}=0.0V resulted in an ideal I-V characteristics, whereas pulsing from a steady state biasing point V_{ds}=0.0V, V_{gs}=-7.0V resulted in a decrease in drain current. This decrease was associated with surface phenomena of the devices such as surface and interface trapping. We passivated the surface of this wafer by SiNx passivation layer and observed a significant improvement in drain current as shown in Fig 2b. In many other cases we recorded a 3-fold increase in output power after passivation. Detailed passivation tests, related pulse measurements and resulting trap related anomalies will be explained at the time of presentation.

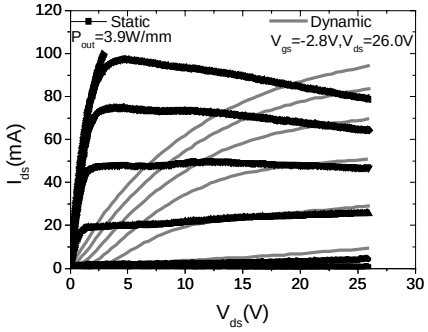
Device design and technology optimisations, mounting and testing at the FBH showed power levels up to 15.1 W at 2 GHz operation. At 2 GHz the maximum power density of 5.2 W/mm scaled linearly with device periphery up to 2 mm. Whereas at 10 GHz, 4.5 W/mm scaled linearly up to 1 mm (Fig. 3 a) and b)) .This non linear power density scaling at larger periphery could either be the result of thermal problems or design parasitics. These issues led us to thermal simulations, which were then performed using Nastran-Patran software package. The reference temperature of an ideally coupled heat sink was 300 K in our case. The simulated channel temperature of 1mm device on SiC valued to 350 K whereas this changed to a value of 365 K in case of 4mm device. Device packaging in CuW increased the temperature to 416 K. Almost similar channel temperature values of 1mm and 4mm devices under ideal heat sinking conditions showed that the nonlinear scaling at larger periphery should not be the result of thermal problems. On the other hand the negative effect of packaging on channel temperature showed the direct dependence of simulation results on heat sinking techniques. This implies that the simulated results could be different under non ideal conditions. The temperature of chuck is not exactly 300 K during practical on wafer measurements but exceed due to presence of air gap in between wafer and chuck roughness. Also a minor change in maximum available gain at 2 GHz confirmed that it was not a design parasitic problem. Hence thermal effects were considered as one of the cause of non linear power density scaling with respect to device periphery at 2GHz. Whereas at 10 GHz the strong decay of maximum available gain (Fig. 3 c)) showed the increased effect of design parasitics with frequency. We therefore believe that both of these factors namely thermal problems and design parasitics were responsible for the decrease of maximum unilateral gain and non linear power density scaling at larger periphery.

Conclusion

We have performed a thorough thermal and electrical study in order to find a cause of power reduction in AlGaN/GaN HEMT devices. Dynamic I/V pulse measurements are proving the trap related anomalies as one of the major obstacles in improving power performance of device. Surface passivation is surely a way to mitigate these anomalies and provide potential enhancements in power performance capability of device. Thermal issues under non ideal heat sinking conditions have been identified as a limiting factor for ultimately high absolute rf-power values even if the devices are fabricated on thermally highly conductive SiC substrates.

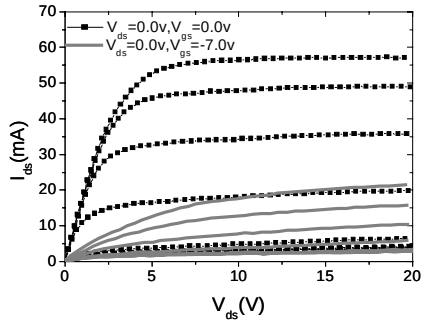


Wafer A

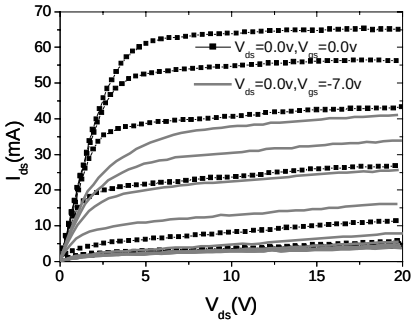


Wafer B

Figure 1: Static versus dynamic I/V-characteristics of different wafers delivering devices with different power density.

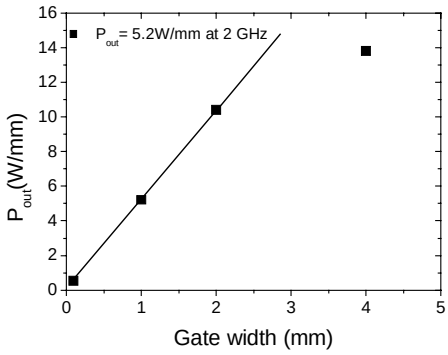


a)

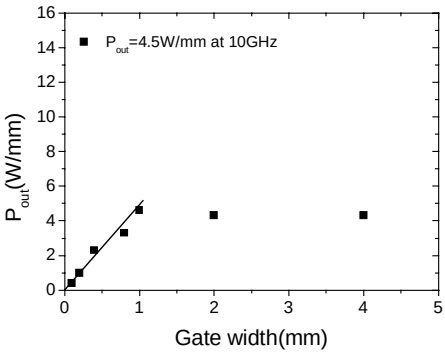


b)

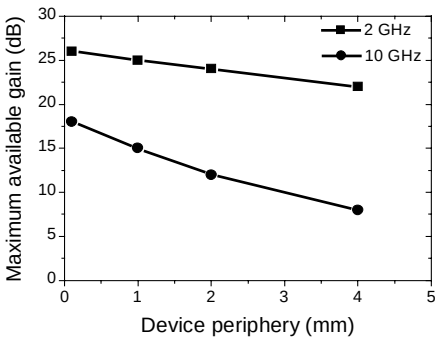
Figure 2: Gate lag effect; a) before passivation, b) after passivation



a)



b)



c)

Figure 3: Microwave properties in dependence on device scaling:

a) Output power versus gate width for 2GHz
b) Output power versus gate width for 10 GHz
c) MAG versus total gate width

Reference:

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Improved HEMT devices from AlGaN/GaN heterojunctions using AlN interlayers

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ABSTRACT

The benefits of introducing low temperature AlN layers into the GaN buffer of AlGaN/GaN heterojunctions are shown through HEMT performances improvement. A comparative study of DC, switching and RF characteristics in improved and in standard HEMTs is presented.

INTRODUCTION

GaN-based heterostructures are very suitable for high-power electronic devices. Despite the improvements in material quality and processing technology, GaN high electron mobility transistors (HEMT) are not yet in the commercial line. The lack of dislocation-free GaN bulk substrates is the main issue, and the use of alternative substrates requires the inclusion of elaborated buffers to lower the final dislocation density. Low temperature AlN interlayers grown by Metal-Organic Vapor Phase Epitaxy (MOVPE), embedded into the GaN buffer, have been shown to block efficiently some of the threading dislocations, and this technology has been used to improve the performance of GaN UV detectors [1]. Concerning AlGaN/GaN heterojunctions, such approach has not been too much explored either by molecular beam epitaxy (MBE) [2], or by MOVPE [3]. We report here on the performance improvements of AlGaN/GaN HEMTs when using buffers with a double AlN interlayer grown by MOVPE technology. A comparative study with standard structures will be shown.

EXPERIMENTAL AND RESULTS

The AlGaN/GaN heterostructures were grown by low-pressure MOVPE on a c-plane sapphire substrate [3], starting with an undoped 2μm thick high-resistivity GaN buffer layer (template), common to both HEMT structures subsequently grown. In standard buffer heterojunctions (SBH), a 1μm thick GaN top layer, and a ~200Å AlGaN barrier were added. The Al mole fraction was in the 0.43-45 range. In the interlayered buffer heterojunctions (IBH), two 30 nm thick low-temperature AlN layers separated by a 0.5 μm GaN layer were first deposited, prior to the growth of the ~1μm thick top buffer and the AlGaN barrier. Two sets of SBH and IBH were grown with approximately the same buffer structure, and AlGaN barrier composition and thickness. AlN interlayers generate a compressive strain in the GaN top most layer, and that situation prevents the AlGaN barrier from plastic relaxation, resulting finally in an enhanced polarization field with respect to standard heterostructures [3,4]. From sheet electron density dependence on gate voltage (n_S^{CV}), IBHs structures showed a higher pinch-off voltage (1V higher), and a 17% higher electron density than SBH HEMTs. Computer simulations were performed to confirm the experimental results [4].

In HEMT processing, Ti/Al/Ti/Au for ohmic contacts (R_c=0.4Ω.mm), Pt/Ti/Au for micron size gates, and Ni/Au for submicron gates were used. Submicron gates were defined by e-beam lithography, being planar stripes (not mushroom-gate). Mesa isolation was made by ion beam

milling (IBM) using Ar ions. Passivation was achieved by SiN layer deposition by plasma enhanced chemical vapor deposition (PECVD). HEMT devices were fabricated in both SBH and IBH wafers. A comparative study of device characteristics (trapping, current collapse, switching and RF) fabricated in both types of wafers will be presented. Device parameters were obtained by driving the gate with 300 μs pulses. I_{dmax} values of 1.5 A/mm, and g_{Mmax} =290 mS/mm were obtained in L_G= 0.2 μm and W_G=75 μm IBH devices. Usually, IBH HEMTs showed at least 20% higher values than their homonymous SBH devices (Fig.1a). Performance degradation was observed increasing W_G due to thermal effects, likely as a result of using Al_2O_3 as a substrate. f_T was taken as figure of merit of the RF measurements for devices with L_G=0.2μm (Fig. 1b), giving an increase ranging from 20 to 77% in each set of samples. Due to technological problems and non optimised layout-device for submicron operation, these devices do not show the real potential of these wafers. More realistic values were found in IBH devices with L_G=1 μm and W_G=75 μm, with f_T = 9.5 GHz and f_{max} =33.4 GHz.

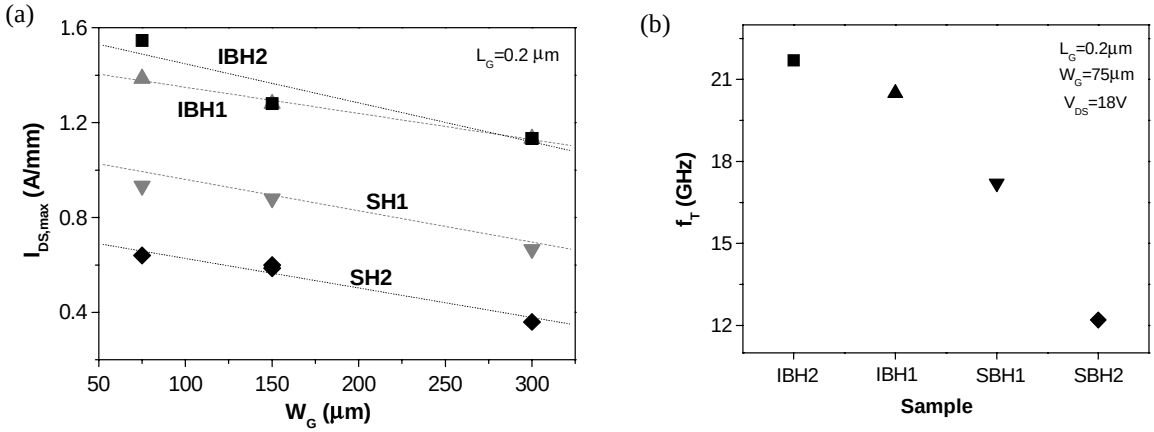

Figure 1.- (a) I_{dmax}, and (b) f_T values in IBH and SBH transistors with 0.2 μm gate length.

CONCLUSIONS

In summary, this work shows the improvements brought by the use of buffer layers containing AlN interlayers in the performance of AlGaN/GaN HEMTs. The increased compressive strain in the GaN buffer prevents the AlGaN barrier from relaxation, resulting in an increase of the total polarization field in the pseudomorphic heterostructure, increasing the transistor channel carrier density and pinch-off voltage. High performance DC parameters (pulsed V_{GS}), and good RF response in 1 μm devices have been obtained.

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Enhancement-Mode $Al_xGa_{1-x}N$/GaN Modulation Doped Field Effect Transistors

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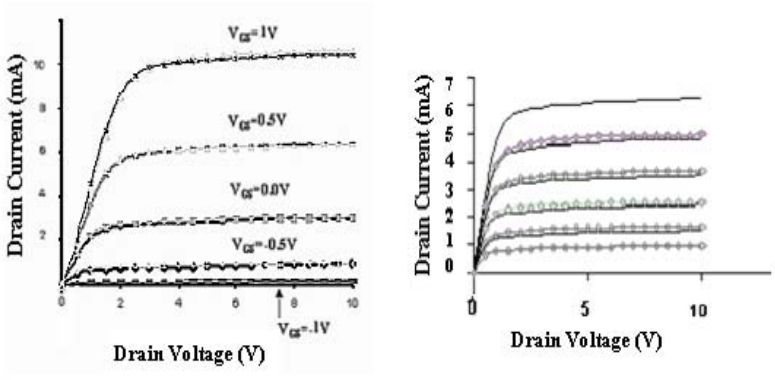
Fabrication and characterization of enhancement-mode (E-mode) AlGaN/GaN Modualtion Doped Field Effect Transistors (MODFETs) are reported using MBE grown material on sapphire. Devices with gate length of 1-μm show threshold-, knee-, and off-state breakdown voltage of 0, 1.5, and 90 V, respectively. The devices demonstrate an extrinsic gate transconductance of 180 mS/mm, which is by far higher than previously reported E-mode AlGaN/GaN MODFETs. A unity current gain cutoff frequency (f_T) of 6 GHz, and a maximum oscillation frequency (f_{max}) of 12 GHz were measured. Load-pull measurements demonstrate a power gain of 6.7 dB at 5 GHz. No current collapse was observable after 10 hours of RF and DC stress.

Developments in wireless communications have drastically increased the need for high-power, high efficiency, linear, low-cost, monolithic solid-state amplifiers in the 1-30 GHz frequency range. While mainstream III-V technologies (i.e., GaAs) fall short of satisfying a majority of these requirements simultaneously, newer materials such as GaN, having superior electronic properties, are deemed to have the capacity to fulfill these requirements. As for AlGaN/GaN MODFETs, with the exception of a few reports [1]-[3], the reported devices are all of the depletion mode (D-mode) type. Attaining an enhancement mode device in GaN technology with a doping-independent polarization based 2DEG, is more difficult compared to other III/V technologies. Despite the possibility of controlling the polarization-based charge of the AlGaN/GaN 2DEG by variation of the barrier thickness [4], realization of both enhancement and depletion devices may be limited by both post-etch surface- and Schottky-quality.

The E-mode MODFET reported in this work was fabricated on an MBE grown AlGaN/GaN heterostructure on sapphire. The heterostructure consists of a 55-nm AlN nucleation layer, followed by a 2-μm GaN channel layer, a 2-nm AlGaN spacer, a 15-nm Si-doped barrier, and a 2-nm cap layer. Unlike other reported AlGaN/GaN E-mode MODFETs, the E-mode operation of the device is not defined through the reduction in barrier thickness which makes the design of the E-mode device less process-sensitive compared to the thinned barrier designs [2].

The fabrication starts with a mesa definition. Mesas of 0.8-μm height are defined using a two stage Cl_2-based RIE etch followed by a pre-ohmic preparation in HCl:$H_2$0 (7 ml : 100 ml) 50 °C solution for 30 seconds. Transistors are then fabricated with Ti/Al/Pt/Au (200Å/800Å/100Å/3000Å) source-drain ohmic contacts. Ohmic contacts are annealed at 700°C in a 410 Heatpulse annealing system for 30sec. Annealing is repeated for 15 more seconds at 725 °C, and a final 15 seconds at 775 °C. Our TLM measurements indicate that after the final stage of annealing the change in the surface potential shifts the operation condition more towards the E-mode operation. Finally, Pt/Ti/Au (500Å/200Å/1500Å) gates are defined after plasma descum and BHF etch. No intentional gate recess is done in the fabrication of E-mode device. The fabricated devices have optically defined 1-μm gates.

This work was supported under contracts N00014-02-1-0128, N00014-01-C-0346, ECS0233500, and HRL Laboratories.



(a) (b)

Fig. 1. (a) Measured pre- and post-RF stress, DC drain current/voltage characteristics for V_{GS} of -1 V to 1 V. The pre- and post-RF stress curves are right on top of each other. (b) DC drain current/voltage characteristics for V_{GS} of -0.4 V to 0.4 V with 0.2V steps. Solid lines are after UV illumination and curves with ◊ symbols are before UV illumination.

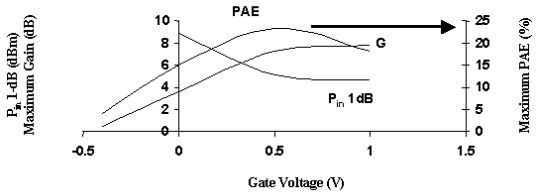


Fig. 2. Measured maximum gain (dB), 1-dB gain compression point (dBm), and maximum PAE (%) at 5 GHz, V_{DS}=10 V, and variable V_{GS}.

The DC characteristics of the fabricated 2×55-μm device illustrated in Fig. 1(a) indicate a good ohmic quality, and a comparatively low knee voltage (less than 2V), which is comparable to the best reported AlGaN/GaN E-mode MODFET. Despite being unpassivated and unlike D-mode AlGaN/GaN devices, the E-mode AlGaN/GaN MODFETs do not show any considerable current collapse. This is demonstrated in Fig. 1 (a) which depicts the drain current/voltage of the 2×55-μm device before and after 10 hours of RF/DC stress, respectively. This device is showing a record high extrinsic gate transconductance of 180 mS/mm (at V_{GS}= 2 V), while having a pinch-off voltage of -0.5V.

Current collapse, so far has been one of the major concerns of the nitride technology [5]. Not having any significant manifestation of current collapse in our unpassivated E-mode AlGaN/GaN MODFET, confirms the role of surface states on the Enhancement-mode operation of this device. Device annealing appears to have modified the surface potential by filling the existing surface states. The virtual gate created by the filled surface states compresses the current level of the normally D-mode device to the levels expected after current collapse. The results obtained by UV illumination, support the assumption of a virtual gate presence. After illuminating E-mode devices with a threshold voltage of -0.5 V, the current level improves by almost a third of its original value at V_{GS}=0 V (Fig. 1(b)) and the pinch off voltage moves toward more negative values by almost -1 V. Unlike the pre-illumination device characteristics the devices after illumination show considerable amount of current collapse when subjected to DC-stress. Load-pull power measurements on AlGaN/GaN E-mode devices were also performed and reported for the first time. Fig. 2 depicts the variation of the maximum PAE, Gain and 1-dB compression point with V_{GS} at fixed drain voltage of 10 V.

In conclusion, high performance AlGaN/GaN E-mode MODFETs is demonstrated. First investigations of the E-mode operation mechanism of these devices by subjecting them to illumination suggest a dual-gate operation mechanism. For the unpassivated E-mode devices, no dispersion effects were observed after 10 hours of DC and RF stress. The fabricated devices show a gain value of 6.7 dB and maximum output power level of about 16dBm at 5 GHz.

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Bias Dependent Frequency Response of AlGaN/GaN HEMT

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AlGaN/GaN heterostructure transistors show potential in high-frequency high-power applications because of their high breakdown voltages and high electron saturation velocities. There was implemented Si_3N_4 passivation of the surface of the devices for improving the RF performance of the device and elimination of the RF power slump. The optimum conditions for the passivation have been established to double the output power of the device. In this paper we report studies of the frequency performance of AlGaN/GaN HEMT. Unity gain cutoff frequency dependence on the gatelength was studied. Measurements were performed at low drain biases. Effective electron velocity under the gate was extracted. Bias-dependent measurements of the unity gain frequency on the device before and after the passivation were performed.

Introduction

Fabrication of AlGaN/GaN heterostructure high electron mobility transistors involves growth of AlGaN/GaN epitaxial structure on the sapphire or SiC substrate, preparation of the sample for processing, mesa isolation step, ohmic contacts fabrication, gate level fabrication, pads level processing, followed by passivation of the device surfaces and air bridging for large periphery devices. The fabrication process developed at Cornell [1] provides repeatable and robust results for all mentioned levels. Typically devices fabricated on SiC substrate show full channel current of 1.1A/mm and devices fabricated on sapphire substrate show full channel current of 0.9A/mm. Measured breakdown voltage is typically 50-80V. Gate level fabrication was calibrated to deposit gates with the length between 0.15um and 0.6um. Fabrication process is similar to process described in [2],[3].

Unity Current Gain Frequency Measurements

After the set of devices with the gatelengths in the range of 0.15um-0.6um was fabricated, the unity current gain frequency was measured for each device. Shown in Fig.1 is the dependence of the cutoff frequency on the gatelength. Effective electron velocity of 10^7cm/sec was extracted from the slope of the curve

$$F_T = \frac{V_{eff}}{2\pi L_g}$$

Bias dependence of the unity current gain frequency was observed. Shown in Fig.2 is the comparison of the unity current gain frequency of the same device before and after the passivation. Drain voltage increase caused decrease of the cutoff frequency. This effect of drain bias became less significant after the passivation of the surface of the device. More pronounced RF power slump at high drain biases in the unpassivated device could be explained by the slump of the gain at higher frequencies with the increase of the drain voltage.

Device Stability

Device DC characteristics greatly depend on the way in which the measurement is performed. The very first current-voltage curves measured after the device has been inactive for long period of time differs significantly from the current-voltage curves collected after some time which is long enough to charge possible defects in the barrier layer and on the surface of the device. The time constants of the traps found in the device are on the order of few milliseconds [4]. Shown in Fig.3 are

current-voltage curves collected from the very first measurement and after multiple measurements on unpassivated device , illustrating charging processes.

Summary

Dependence of the unity current gain frequency on the bias conditions was observed. The drain voltage of the device was varied from 5V to 35V. The cutoff frequency drop could not be explained by the drop of the two-dimensional gas mobility due to the device heating only. Charge leaking from the gate at high drain biases is trapped in the barrier layer of the device, depleting charge in the channel and increasing effective gatelegth. After the device passivation surface leakage current is increased due to introduction of the low conductive passivation film on the surface of the device. Electric field in the barrier layer near the gate is relaxed as the effect of surface passivation. Less charge is accumulated near the gate in the barrier.

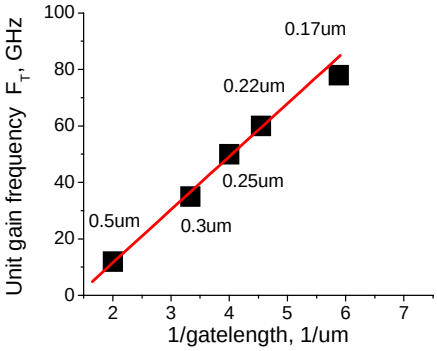

Figure 1. Frequency scaling with the gatelength at Vds=5V, Vgs=-3V

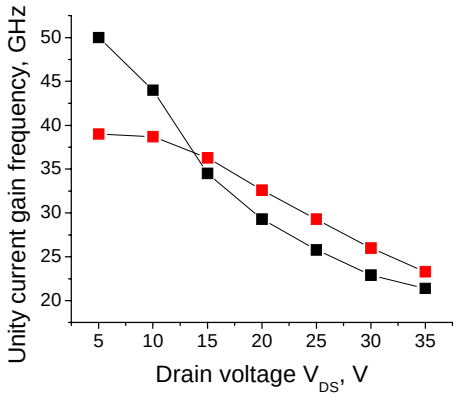

Figure 2. Bias dependent unity current gain frequency of unpassivated and passivated devices

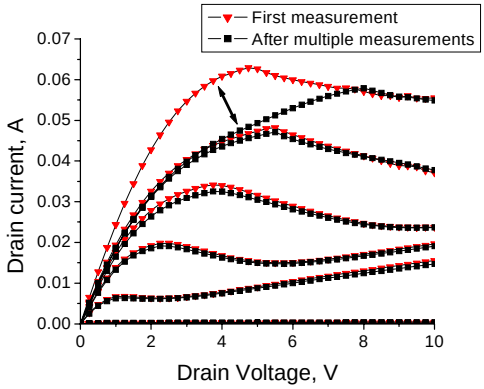

Figure 3. DC curves from the very first measurement and after multiple measurements

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Behavioural Model For AlGaN/GaN HEMTs on Sapphire and SiC Constructed From Multi-Bias Large-Signal Measurements

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Abstract — AlGaN/GaN HEMTs have a high potential for high-power applications at microwave frequencies. To enable circuit design, we developed a behavioural model for devices based on both sapphire and SiC substrates. The models are based on time-domain large-signal measurements and are valid for a wide range of DC operating conditions at selected loads.

I. Introduction

GaN-based devices are extensively being pursued for applications in high-power microwave circuits [1]. Specific physical characteristics, such as temperature dependency, render the application of 'classical' modelling techniques, among which direct extraction, difficult. In this paper, we describe the construction of a behavioural model. This approach has as advantage that it is based on measurements only and consequently that the precise equivalent scheme does not need to be known. The method's theoretical background has been described earlier [2]. In this paper, we apply the method to GaN HEMTs on sapphire and SiC substrates, and generate a model valid over a wide range of biases.

II. Model Construction

The modelling method [2] involves that a microwave two-port device can be described by:

$$\begin{aligned} I_1(t) &= f_1\left(V_1(t), V_2(t), \dot{V}_1(t), \dot{V}_2(t), \ddot{V}_1(t), \ddot{V}_2(t), \cdots, \dot{I}_1(t), \dot{I}_2(t), \cdots\right) \\ I_2(t) &= f_2\left(V_1(t), V_2(t), \dot{V}_1(t), \dot{V}_2(t), \ddot{V}_1(t), \ddot{V}_2(t), \cdots, \dot{I}_1(t), \dot{I}_2(t), \cdots\right) \end{aligned} \quad (1)$$

with $I_1(t)$ and $I_2(t)$ the terminal currents, $V_1(t)$ and $V_2(t)$ the terminal voltages, and the dots representing (higher order) time derivatives. The objective of the modelling technique is to find the number of independent or state variables, and consequently to determine the relationships $f_1(.)$ and $f_2(.)$.

The first step is collecting time-domain data at operating conditions that are realistic for the device use. The fundamental frequency is fixed to 4 GHz. We performed power-swept single-tone measurements using an LSNA [3] at gate voltages near V_T and near maximal g_m, and at drain voltages ranging between 2 V and 20 V. Since AlGaN/GaN HEMTs have little or no gain when measured with a 50 Ω load, we extended our set-up with a passive tuner and repeated this set of measurements for selected load conditions. This enables us to have a model that is valid over a wide range of DC operating conditions and at loads, realistic for circuit applications.

The next step consists in determining the independent (or state) variables. Since we are considering a HEMT, we can easily estimate that a good set of state variables be the terminal voltages, and the corresponding first and second order time derivatives. As it is known that AlGaN/GaN HEMTs are susceptible to temperature effects, we add the net dissipated power P_{net}, being a good measure for the actual device temperature [4], as 7th independent variable.

Subsequently, the functional relationships $f_1(.)$ and $f_2(.)$ can be determined. This is done by fitting the measured time-domain terminal currents towards the independent variables. The terminal voltages are measured, while the derived quantities, like the first and second order time derivatives, are calculated from the measurements. As fitting function, we adopted the use of artificial neural networks (ANNs). The ANN topology is limited to one hidden layer and the considered activation function is the sigmoid function, due to its well-defined and smooth asymptotes. The ANN is trained using the back-propagation algorithm, as implemented in the NeuroModeler program [5].

III. Modelling Results

We considered 2 devices: device A is a 100*1.5 μm^2 AlGaN/GaN HEMT on sapphire; device B is a 300*0.3 μm^2 AlGaN/GaN HEMT on SiC. Both device types have been fabricated by IEMN [6]. Table 1 lists the results of the ANN training. The correlation coefficient is a measure for whether we selected

the right set of independent variables. Two alternatives are considered: Case 1 is the model with 6 state variables included, whereas case 2 is the model with 6 + 1 (=P_{net}) state variables. The error levels are low for both device types, and the high correlation denotes that we have a good set of independent variables. We also notice only a marginal improvement when P_{net} gets included.

Table 1: Overview of the ANN training results.

	Device A				Device B			
	Case 1		Case 2		Case 1		Case 2	
	I_1	I_2	I_1	I_2	I_1	I_2	I_1	I_2
correlation	0.9972		0.9982		0.9989		0.9997	
average error [%]	1.12	1.48	0.98	1.13	1.12	2.19	0.82	0.93

Finally, we implement the models in a microwave circuit simulator. Figures 1 and 2 compare simulation results to measurements. We notice that the agreement is very good, even for an operation condition in pinch-off and at a low drain voltage (left plots).

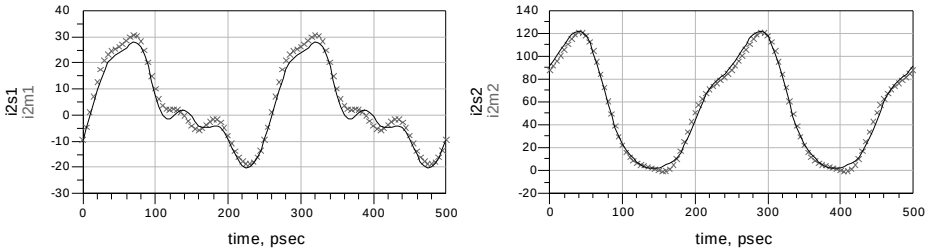

Fig. 1. Device A: comparison of the measured (x) and modelled (solid line) I_2 [in mA] at 2 operating conditions (left: V_{gs}=-3 V, V_{ds}=2 V, P_{in}=21 dBm, Z_{out}=24+j99 Ω; right: V_{gs}=1 V, V_{ds}=20 V, P_{in}=22 dBm, Z_{out}=55+j76 Ω).

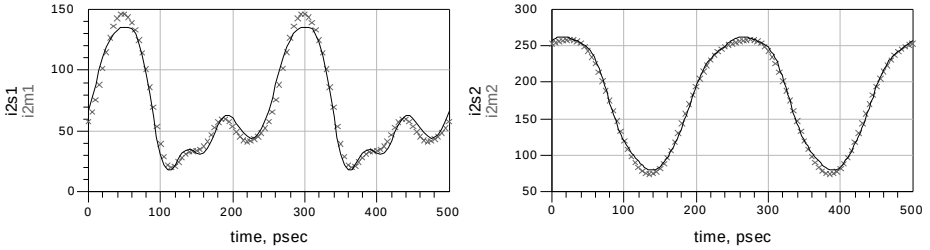

Fig. 2. Device B: comparison of the measured (x) and modelled (solid line) I_2 [in mA] at 2 operating conditions (left: V_{gs}=-2 V, V_{ds}=5 V, P_{in}=17 dBm, Z_{out}=66+j70 Ω; right: V_{gs}=0 V, V_{ds}=20 V, P_{in}=17 dBm, Z_{out}=55+j7 Ω).

IV. Conclusion

We constructed an accurate behavioural model for AlGaN/GaN HEMTs from multi-bias time-domain large-signal measurements at several loads. We noticed that for the considered device sizes the improvement in model accuracy is marginal when including the temperature-dependency, and this for AlGaN/GaN HEMTs on both sapphire and SiC.

Acknowledgement

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Millimeter-Wave MMICs - Current Activities and Trends

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Abstract

PHEMT based millimeter-wave MMICs on GaAs-substrate have been in the scope of research during the last years. Particular interest has been spent on circuits and systems for communication and sensor applications. Examples are integrated automotive sensors at 77 GHz and local multipoint distribution systems (LMDS). The most interesting developments in these fields will be reviewed with respect to technology, circuit and system design. Current trends and aspects of future integration technologies will be discussed, too.

Introduction

Cost is the primary focus in the new millennium. The increasing market in wireless communications and automotive sensor applications demands high volume and low cost millimetre-wave MMIC (MWMMIC) and multi-chip module (MCM) technology. In the 1990's great expenses were made towards the development of a highly reliable, high yield GaAs PHEMT-MMIC-technology for automotive radar systems operating in the 76-77 GHz frequency band [1], [2], [3]. During this time the mainstream of the developments went towards complete monolithic solutions of the 76/77 GHz front-end. However, cost expensive GaAs chip area and progress in millimeter-wave flip chip MCM technology have been led to new constraints. Currently, mixed chip sets in combination with flip chip technology seem to match the cost requirements best [4], [5], [6], [7].

Parallel to cost reduction of the system, system performance has been increased continually. State of the art technology with respect to system performance, devices, circuits and interconnects will be the focus of the discussions.

System

A simplified example for the system topology is given in Fig. 1. A VCO MMIC generates the 77GHz signal. A fraction of the VCO power is down converted by the DRO/SMIX combination for being processed in the PLL circuit. SMIX is a subharmonically pumped mixer using the 5th LO-harmonic for the mixing process. The transmit MMIC contains a multistage amplifier, a power splitter and a few medium power amplifiers, which feed a common dielectric lens. Depending on system requirements, up to 5 medium power amplifiers (MPAs) have been used to obtain the narrow transmit/receive beams required for a high angular resolution. For the down conversion of the receiving signal resistive PHEMT Mixers have been applied as well as Si-Schottky diode mixers.

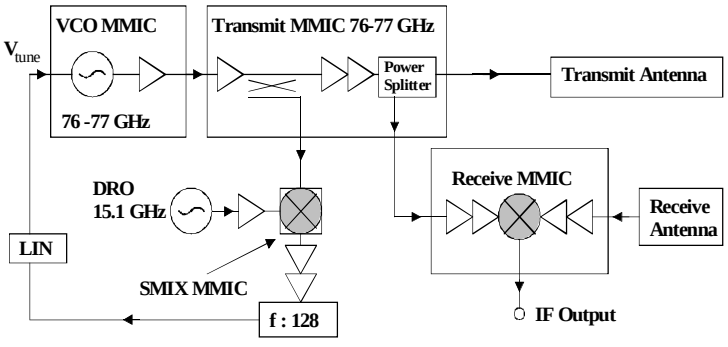


Fig. 1: Topology of the FMCW Radar Front-End.

Main System Specifications:

- Measurement range
  - Distance 1 – 150 m
  - Direction +/- 5°
  - Velocity +/- 200 km/h
- Multiple target capability
- Frequency Range 76 – 77 GHz
- Temperature range -40…+105°C

PHEMT-Technology, Modelling

The MMICs have been fabricated by using the Infineon PHEMT 110 process technology. The cross section of the GaAs PHEMT is given in Fig. 2. The process technology has been optimised with respect to low production costs or in more detail, with respect to high production throughput, high yield, and high reliability. Thus, 6'' wafers and optical stepper lithography have been applied instead

of electron beam lithography. The main features of the process technology are given in the following tables.

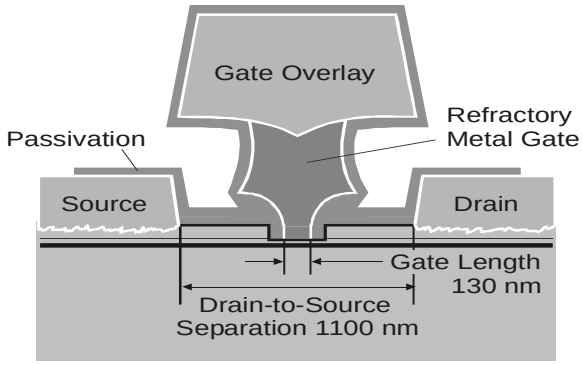


Fig. 2: Cross Sectional View of a GaAs PHEMT [7].

Main Features:

- Double heterostructure GaAs PHEMT
- 130 nm gate length
- 6- inch MBE wafers
- Optical lithography with I-line wafer stepper
- Gate fabrication by sidewall spacer process
- Ohmic metal self- aligned to gate
- MIM capacitors, epi resistors
- 3 interconnect metal layers incl. Air bridges

Main DC Parameters:

- Pinch- Off Voltage	-0.5 V
- Maximum Drain Current	650 mA/mm
- Maximum Transconductance	700 mS/mm
- Gate to drain Breakdown Voltage	4 V

Main RF Parameters:

- f_T	110 GHz
- f_{Max}	> 200 GHz
- Fmin	0.6 dB
- $P_{out, Max}$	150 mW/mm

A modified Angelov PHEMT model [8] has been used for the design process, extended with respect to non-linear and noise behaviour [9], [10] and implemented into the CAE tool ADS™.

MWMMICs

A) Coplanar technology

Coplanar waveguide technology has been used because of cost (processing is simplified - no wafer thinning, no via holes) and because of further impressive advantages: ground parasitics and frequency dispersion are lower than for comparable microstrip technology, less chip area is required and inexpensive on wafer characterisation is possible. Models for coplanar waveguides and discontinuities according to [11], [12] have been used and implemented in our design environment.

B) VCO

There are two basic circuit topologies for oscillators with active three-terminal devices: negative resistance topology and feedback topology. While the feedback oscillator concept is primarily used in the frequency range up to 1 GHz most of the microwave and millimetre-wave oscillators apply the negative resistance concept. However, it has been shown [13] that also with the feedback concept excellent results are achievable in the millimetre-wave band, which are partly superior to those, achieved with negative resistance concepts [3]. The experimental results obtained with the W-band feedback oscillator are summarised in the table below.

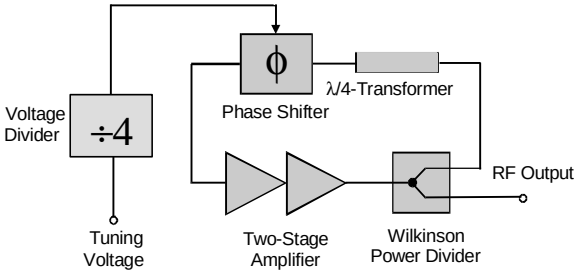
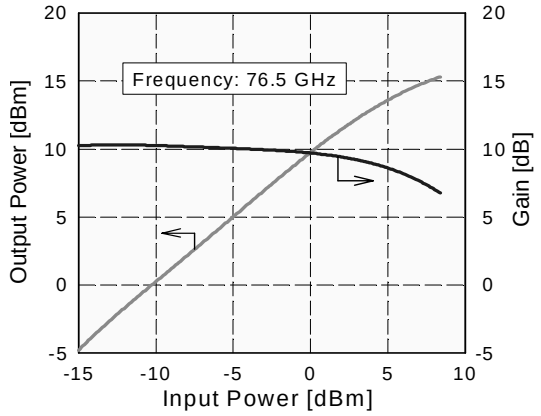


Fig. 3: 74 – 78 GHz Feedback Oscillator Topology [7].*l*

Experimental Results:

- Center Frequency	74…78 GHz
- Tuning Bandwidth	2 GHz
- Output Power	7.5 dBm
- Outp. Power Variat. vs. Freq.	± 1 dB
- Phase Noise /1 MHz Offset	-78 dBc/Hz
- Frequency Drift vs. Temp.	6 MHz/°C
- Output Power Drift vs. Temp.	0.02 dB/°C
- DC Power Consumption	130 mW

The MPAs are used for various functions within the radar frontend as, for example, a buffer amplifier for the VCO, a LO amplifier for the receiver mixer, or a transmitter building block. Several medium power amplifiers (MPAs) have been designed in the course of the project [3], [5], [14]. The main features of the MPA of the latest generation are provided in the table below. The goal specifications have been obtained during the optimisation process of the system performance:



MPA Main Features (76,5 GHz):

- Two Stage Design	
- Unconditionally Stable	
- Output Power (1 dB Compr.)	>12 dBm
- Gain	>10 dB
- Input Return Loss	>10 dB
- Output Return Loss	>10 dB
- Power Consumption	240 mW
- Chip Size	0.9 x 1.69 mm

Fig. 4: Measured MPA Gain and Output Power [5].

D) Mixers

Two types of mixers have been developed: harmonic mixers for the stabilisation loop of the VCO and receive mixers for the receive path. Various concepts have been studied: diode mixers, active and passive FET mixers, monolithic and hybrid mixers. In the following, only monolithic mixers will be discussed.

A subharmonically pumped gate mixer MMIC using the 5th LO harmonic for the mixing process has been developed for the VCO stabilisation [15]. A conversion loss down to 18 dB has been achieved at 10 dBm LO power (Fig. 5). This result was about 10 dB better as a former one obtained with a comparable diode mixer MMIC.

For the receive path diode type and resistive mixer MMICs have been developed [16]. Both mixer types show a comparable conversion loss. However, because of no dc-current flow, the resistive mixer shows significantly improved low frequency noise behaviour.

Considerably better low frequency noise values than with resistive GaAs PHEMT mixers have been achieved with hybrid Si Schottky diode mixers. A lot of research has been spent into the understanding of low frequency noise mechanisms of resistive mixers, too [17]. These developments will be discussed at the workshop.

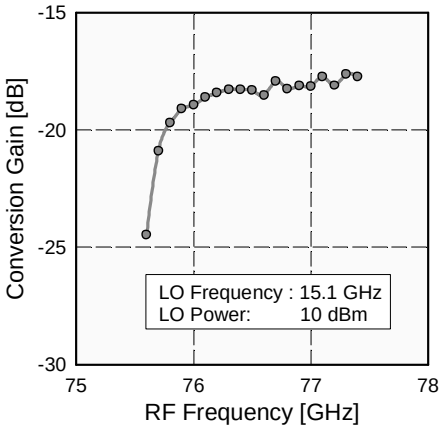


Fig. 5: Conv. Gain of the subharmonically Pumped Mixer MMIC versus RF Frequency [3].

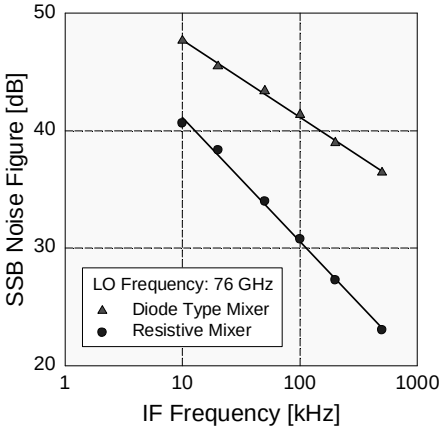


Fig. 6: Low Frequency Noise Figure of Resistive and Diode Type Mixer MMICs [3].

Conclusions

A variety of achievements in the field of MWMMIC development for sensor applications has been discussed. With respect to cost and system requirements, a well-balanced mixture of monolithic and hybrid integrated circuits seems to be the best solution. A highly precise and reliable millimetre-wave interconnects technology like flip chip technology is necessary in this case in order to sustain the system performance.

Acknowledgement

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The author likes to thank Dr. H.-J. Siweris from the millimeter wave group of Triquint Semiconductors, Munich, for valuable discussions.

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Silicon Germanium- The Communications Technology for Today and Tomorrow

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ABSTRACT

In this paper we highlight the effectiveness and flexibility of SiGe BiCMOS over a wide range of performance and applications. Process customization is done to provide high quality passives, which greatly enables fully integrated single chip solutions. Product examples include 40 Gbps (OC768) components using high-speed SiGe HBTs, power amplifiers (PAs), integrated voltage controlled oscillators (VCOs), and very high level mixed-signal integration. It is argued that such key enablement make SiGe BiCMOS the communications technology for today and tomorrow.

INTRODUCTION

With the dawn of internet, the communication market segment has seen an explosive growth. SiGe BiCMOS technology provides a very elegant solution to address these markets for various reasons:- (a) high-speed HBTs provides comparable f_T, f_{MAX}, linearity (IP3), and noise figure (NF_{min}) compared to more exotic HBTs like GaAs and InP, (b) multiple variants of HBTs that are doped selectively to provide varying breakdown voltage requirements can be seamlessly integrated with state-of-the-art CMOS and high quality passives, and (c) provides higher yields and lower cost compared to other viable technology options. IBM's SiGe BiCMOS is now in its fourth lithographic generation since the introduction of the 0.5 µm generation into volume production. The key component of the device offering is the SiGe-base HBT whose performance (f_T, f_{MAX}) has been significantly improved to over 200 GHz in the 0.13 µm generation, see Figure 1. Wireless and storage applications continue to leverage the 0.5 µm and 0.25 µm generations where cost and time-to-market drive the technology choices. In contrast, network communication space leads the 0.18 µm and 0.13 µm product applications where VLSI chips need substantial CMOS integration along with the high performance SiGe HBT. This paper reports IBM's recent SiGe BiCMOS technology enhancements, such as, high-speed HBT development, HBT modifications to address PA application, and high-performance passive element integration, and the key products and applications that these technologies have addressed.

SiGe HBT DEVELOPMENT

SiGe HBT performance improvements in the first three generations of HBT were achieved by structural enhancement including shrinking the emitter width and reducing intrinsic layer thickness. Vertical profile scaling include increasing the base drift field by simultaneously increasing the Ge ramp and reducing the as-deposited basewidth, adding carbon to decrease base diffusion, and reducing the thickness of the collector epitaxial layer. For the 0.13 µm generation, further performance improvement was achieved by adopting a new device structure that significantly reduces base resistance at the same time as increasing f_T without increasing C_{CB} above the prior generation [1]. As shown in Figure 2, this 0.13 µm generation HBT has achieved room temperature operation of a conventional ECL ring oscillator with a minimum stage delay of 4.2 ps for approximately 250 mV output swing. To our knowledge, this is the lowest reported delay for an ECL gate fabricated using transistor devices.

PASSIVE ELEMENTS

Further integration advantages of SiGe BiCMOS can be exploited through improvement in passive elements. Resistors with precision tolerance (+/-6% as 3-sigma) and reduced parasitics, have been achieved with a TaN thin film resistor (~61 Ω/sq.) that is integrated above the metal-1 dielectric. These precision resistors provide the advantage of having low parisitic coupling to the substrate and can be used in the high-frequency signal path as 50 Ω terminations. Highly reliable and high density MIM capacitors have been developed using PECVD nitride films. A novel integration scheme is used for parallel capacitors with capacitance densities as high as 4.0 fF/µm^2. These devices have a Q of 150 at 2 GHz, a very low TCR of 14.5 ppm/C, and is highly linear (voltage coefficient of 4 ppm/V). The performance of spiral inductors has been improved by thickening the spiral metal level and substituting Cu for Al to reduce series resistance.. A dual metal inductor using a thick Al top metal and a low resistance Cu wire and via level directly below it have been implemented in recent technology. This configuration allows for very high Q inductors reaching a

peak Q of 28 for a 1.1 nH inductor at 3.5 GHz. Varactors are critical devices that are important for VCO designs. It is important to have varactors with high linearity, good tunability, and high Q. In order to simplify the device design, one typically designs a varactor utilizing the parasitic process elements in the technology. Typically, such a device does not provide the optimal solution for a varactor design. One can overcome the typical tradeoff between linearity and tuning range for standard varactors by a semi-custom junction varactor that requires one extra implantation mask level. A hyperabrupt junction varactor (HA) has been developed with a fairly large capacitance tuning ratio of 3.0 (Cmax/Cmin) achieved over 0.4V to 2.4V voltage range and excellent Q (<3:1 tuning ratio with Q~50 at 10GHz).

PRODUCT APPLICATIONS

I. Power Amplifiers

Power Amplifiers (PAs) are a core component in the high-growth wireless communications industry. Bipolar transistors are the critical building block of a PA, with silicon, SiGe, and GaAs technologies competing as the technology of choice. A challenge faced by SiGe-based PA technologies is providing sufficient high-voltage immunity without compromising PA performance. We have demonstrated a 0.5 μm SiGe BiCMOS technology where a non-uniform collector design has provided a significant improvement in HBT ruggedness while maintaining a performance suitable for PA development across several different wireless standards. A very high breakdown SiGe HBT (BV_{CBO} > 20V) with f_T > 25GHz has been developed using a shallow retrograde collector that has been successfully utilized for PA applications [2]. A quad-band RF power amplifier has been fabricated which consists of two amplifiers on the same chip: one for GSM 850 / 900 and the other for DCS 1800 / PCS 1900. Its highly integrated, single-ended design has allowed minimum external component count and efficient operation from a single +3.5V power supply. The output power and efficiency characteristics of the PA for 900MHz are shown in Figure 3, indicating sufficiently high efficiency even at higher output power levels. The constant current gain as a function of temperature together with the high current density and low thermal resistance of the PA SiGe HBT technology makes it possible to make use of smaller output devices thereby minimizing parasitic effects. Output power is +31.5 dBm for GSM850, +35 dBm for GSM900, +32.5 dBm for DCS1800 and +32.5 dBm for PCS1900. Power added efficiency in each band is 40%, 55%, 50% and 45% respectively [3].

II. Integrated Voltage Controlled Oscillators

Fully integrated VCOs are a major bottleneck for system-on-chip (SOC) realization of wireless transceivers. High quality passives and high-performance varactors are required for the design of high performance VCOs. VCO parameters requiring high performance passive elements are phase noise, frequency tuning, and VCO gain variation. The VCO gain variation, determined by the linearity of the varactor, has to be minimized since it has an overwhelming influence on the phase locked loop (PLL) performance. By doing so, the PLL loop bandwidth can be maintained relatively constant which will benefit the consistency of the PLL locking time and the phase noise of the PLL. A tri-band GSM direct conversion system requires the VCO bandwidth to be about 10.5%. To cover this 10.5% frequency range over process and temperature variation, more than 20% of the frequency tuning range needs to be designed in the VCO. The standard CB junction varactor offered in our SiGe 5HP technology has a capacitance ratio of Cmax/Cmin=1.45 for a tuning voltage of 0.4V to 2.4V. With fixed capacitances from other active and passive devices unavoidable in the VCO circuit, this 20% frequency tuning range is very difficult to be achieved by the varactor, which is one of the major reasons that multiple band topology is utilized. Using the HA varactor, a large bandwidth VCO is easily designed. In order to benchmark the advantage of these new passive devices in a VCO design, an integrated VCO has been re-designed using the dual metal inductors and HA varactor without any topology change. The original device was designed using a single thick Al layer for inductors and the standard CB junction varactor. The phase noise is improved by more than 2 dB with a 10% saving on power consumption. The VCO frequency tuning range is expanded to 24% from 21% and the VCO gain variation is reduced by 35% over the overall frequency tuning range [4].

III. 40 Gb/s (OC768) MUX/DEMUX

Multiplexing and demultiplexing functions make best use of the integration capability available in SiGe technologies. As an example, a 16:1 multiplexing part with de-skew mechanism on the 2.5 Gbit/s parallel input has been designed by AMCC and fabricated in IBM's 0.18μm 120 GHz SiGe BiCMOS 7HP technology [5, 6]. This part integrates approximately 50,000 CMOS devices, 18,000 SiGe HBT devices, and 10,000 passive devices onto a single chip fabricated. A fully functional and OC768 compatible 4:1 MUX

and 1:4 DEMUX were built using the BiCMOS 7HP technology. The MUX circuit block takes four parallel single-ended data at its input and uses a half-rate clock frequency, e.g. 20 GHz for 40 Gbit/s operation. This chip incorporates about 560 SiGe HBTs, and current consumption is 410 mA from a -3.6V supply voltage. The DEMUX circuit also uses a half-rate input clock for the first 1:2 demultiplexing stage and incorporates about 540 SiGe HBTs. This chip consumes 430 mA from a -3.6V supply voltage, with 40% of this current consumed in the input and output buffers. Both circuits were packaged and tested by connecting back-to-back through their serial interface.

FUTURE TRENDS IN INTEGRATION

Commercial examples of SiGe BiCMOS where the application frequency is less than 2.4 GHz are prevalent today and 5 GHz applications are coming to market. For applications above 10 GHz, however, GaAs based technologies has been the primary choice up to now. Since the frequency range between 20 and 30 GHz is of growing interest for communications and sensor systems, the ability of SiGe to address these applications is important. The feasibility of the 0.5µm BiCMOS 5HP SiGe process for use in MMIC circuits up to 20 GHz has been investigated. Results comprise a 20 GHz 40 mW medium power amplifier and a 19 GHz VCO [7]. It has long been the promise of SiGe BiCMOS that RF analog circuits could be merged with highly integrated digital CMOS. Recently, a very highly integrated chip has been produced in IBM's 0.18µm SiGe BiCMOS 7HP which included over 7 million CMOS transistors and an RF analog block (see Figure 4). Ultimately >90dB of noise isolation was observed between circuit blocks during functional testing.

CONCLUSION

SiGe BiCMOS technology has shown to be an extremely effective and flexible technology platform. Its most obvious advantage over other platforms is the ability to integrate different functions on a single chip. Additionally, careful engineering of the vertical profile of the NPN transistor enables the fabrication of devices suitable for both the high voltage, rugged environment of power amplifiers as well as the absolute highest speed devices (f_T >200 GHz), required for communications today and tomorrow.

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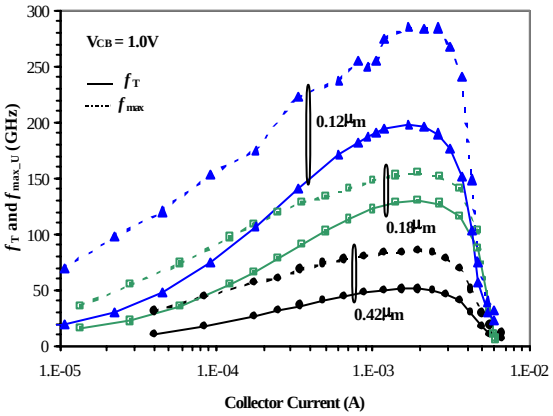

Figure 2. SiGe HBT f_T / f_{max} performance comparison by generation.

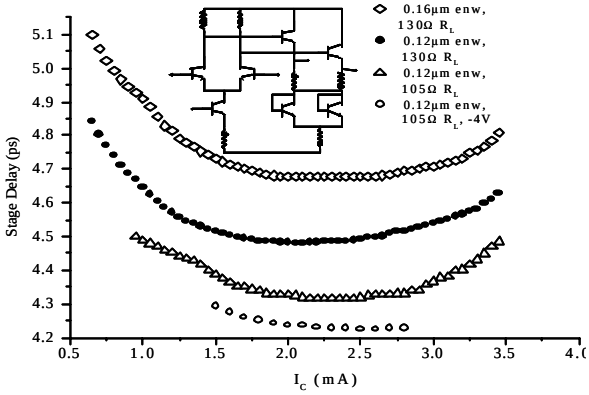

Figure 1. Stage delay vs. collector current (tail current) for ring oscillat fabricated with 0.12 and 0.16 µm emitter width NPN and different load resistors (R_L).

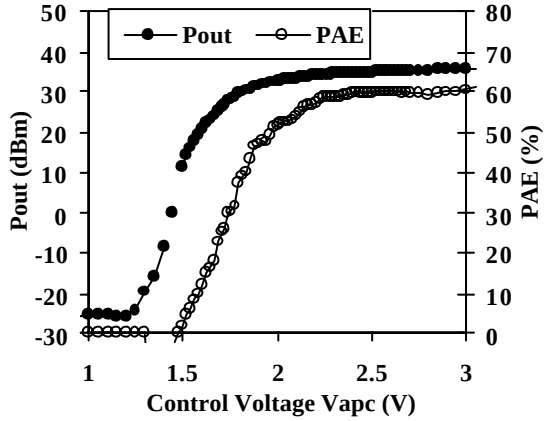

Figure 3. GMSK PA characteristics showing output power and power added efficiency (PAE) at 900MHz and Pin=8.5dBm.

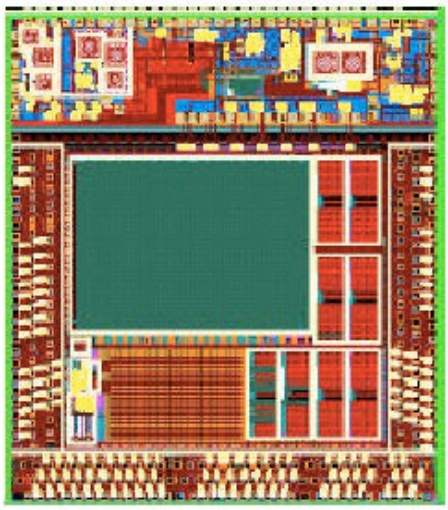

Figure 4. Layout example of a highly integrated system-on-chip

Equivalent Circuit Modeling of GaAs/AlGaAs VCSELs and its Application to the Design of a SiGe Laser Driver

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***Abstract* — We report on the extraction of equivalent circuit parameters of high-speed $GaAs/Al_xGa_{1-x}As$ Vertical-Cavity Surface-Emitting Laser diodes (VCSELs). From on-wafer DC and S-parameter measurements, a simple large-signal model is extracted which describes the electrical behaviour of the laser diode. Using this model, a laser driver IC for 10 Gbit/s datacom applications has been designed using a production-line SiGe-HBT technology.**

I. INTRODUCTION

A VCSEL is a semiconductor microlaser diode that emits light in a cylindrical beam vertically from the surface of a fabricated wafer which offers significant advantages when compared to the edge-emitting lasers currently used in the majority of fiber optic communications devices [1, 2]. In this paper we focus on the modeling of cost-efficient state-of-the-art oxide-confined GaAs/AlGaAs devices with 850*nm* emission wavelength to be employed in 10 Gbit/s optical datacom systems. Only low voltage swings of less than $1V_{pp}$ are required to switch the VCSEL from off-state (slightly above the threshold current) to on-state (few mA). This allows the laser driver to be realized in low-cost SiGe-HBT or even CMOS technology.

II. MODELING

DC current-voltage traces and 1-port S-parameters up to 20 GHz of three different lots have been measured on-wafer for different forward bias currents using a parameter analyzer and an HP8720 vector network analyzer. First the DC characteristics have been fitted to the Shockley diode equation [3],

$$I = I_S \cdot exp[(U - R_{S,dc} \cdot I)/(N \cdot V_T)] \tag{1}$$

where due to forward bias conditions the term '$-I_S$' has been omitted. U is the DC voltage applied to the VCSEL from the anode to GND. This allowed for the extraction of the parasitic DC series resistance $R_{S,dc}$, the ideality factor N, and the saturation current I_S. Due to high recombination (mainly due to stimulated emission) N was in the range of 2-4. From eq. (1) the differential resistance results as $R_{diff} = \frac{dU}{dI} = R_{S,dc} + \frac{N \cdot V_T}{I}$ which is the sum of the parasitic DC series resistance $R_{S,dc}$ and the dynamic diode resistance. This value can be seen in the Smith chart at zero frequency (Fig. 1, left). Plotting R_{diff} obtained from S_{11} versus 1/I allows for the extraction of $R_{S,dc}$ and N as well. We obtained similar data from DC and S-parameter measurements. From the Smith chart in Fig. 1, a capacitive RF behaviour of the VCSEL becomes apparent, which is reflected by the equivalent circuit in the center, where the capacitances C_P and C_D refer to the bond pad and the internal diode, respectively. R_S is the the DC resistance of the distributed Bragg reflector and R_D the resistance of the diode itself.

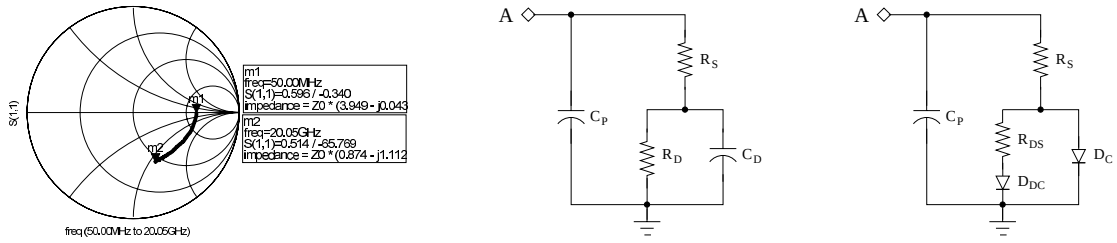

Fig. 1: Measured S_{11} of a VCSEL (left), small-signal equivalent circuit (center) and large-signal model (right).

For high frequencies ($\omega \to \infty$), the pad capacitance C_P and series resistance R_S can be extracted from the admittance Y of the small-signal equivalent circuit as

$$Y_{(\omega\to\infty)} = j \cdot \omega \cdot C_P + \frac{1}{R_S} \quad \to R_S = \frac{1}{Re\left[Y_{(\omega\to\infty)}\right]} \quad \text{and} \quad C_P = \frac{Im\left[Y_{(\omega\to\infty)}\right]}{\omega} \tag{2}$$

Writing the admittance as

$$Y = j\cdot\omega\cdot C_P + \frac{1+j\cdot\omega\cdot R_D\cdot C_D}{R_D+R_S}\cdot\left[\frac{1}{1+\frac{j\cdot\omega\cdot R_S\cdot R_D\cdot C_D}{R_S+R_D}}\right] \tag{3}$$

and performing a Taylor series expansion of the last term using $\frac{1}{1+\mu}\approx 1-\mu$ we get in the limit $\omega\to 0$

$$R_S+R_D=\frac{1}{Re\left[Y_{(\omega\to 0)}\right]} \quad \text{and} \quad C_D=\left[\frac{Im\left[Y_{(\omega\to 0)}\right]}{\omega}-C_P\right]\cdot\left[1+\frac{R_S}{R_D}\right]^2 \tag{4}$$

This allows for the extraction of all elements of the small-signal circuit of Fig. 1 (center) for all forward bias currents, which are then used as the starting values for a final fit to the measured S_{11} in a commercial S-Parameter optimizer. Plotting these results versus the bias current confirmes the physical nature of the equivalent circuit of Fig. 1: While both C_P and R_S remain constant, the diode capacitance C_D increases with current due to the space charge effect and R_D decreases according to $R_D = R_{S,dc} - R_S + \frac{N\cdot V_T}{I}$. This leads to the large-signal model of Fig. 1 (right): The increasing capacitance of C_D with current is modelled using the built-in equation $C = C_{j0}/(1-V/V_j)^m$ of the SPICE diode D_C. Here V is the voltage drop $R_D/(R_S+R_D)\cdot U$ across C_D, and C_{j0} and m are fitting parameters. Note that there is no current flowing through D_C. The decrease of R_D with current is modelled using diode D_{DC}. No capacitive effects are associated with D_{DC}, so $C_{j0}=0$ for this diode. Typical values for a VCSEL with $7\mu m$ active diameter and $0.83mA$ threshold current are $C_P = 80\,fF$, $R_S = 115\Omega$, $R_{DS} = 55\Omega$, $I_S = 11.7\,pA$ with $N = 2.4$ (for D_{DC}) and $C_{j0} = 40\,fF$, $V_j = 8.6V$ and $m = 9.4$ (for D_C).

III. Circuit Design

The standard circuit used to drive edge-emitting laser diodes at bit rates of less than 10 Gbit/s connects the laser with the anode to the supply and sinks the current from the cathode into the driver circuit. In addition to the required broadband RF blocking of the supply, the lengths of several critical bond wires need to be minimized. If such a circuit were used to drive a VCSEL, the cathode would be modulated, which, however, is associated with a large parasitic capacitance to GND due to the use of a doped n GaAs substrate. In order to avoid that, we used the circuit depicted in Fig. 2 on the left. With this topology, only one critical bond wire needs to be taken care of. Since the laser diode is operated with the cathode connected to GND, mounting and heat removal are simplified. The differential pair Q_3, Q_4 converts the balanced signal voltage into a current. When V_{in} is high, Q_4 is off and Q_3 switches the current from Q_6 to the supply through R_{L1}. The current through the VCSEL is then at its maximum and given by the voltage drop across R_{L2}. When V_{in} is low, Q_4 is on and the current of Q_6 compensates the current through R_{L2} partly. The remaining difference current defines the minimum drive current and can be varied by adjusting V_{bl}. Since a bipolar differential pair has a high input capacitance, driving from a 50 Ω source would result in a lowpass behaviour. In order to increase the bandwidth, an emitter follower buffer $Q1, Q2$ with low output impedance was added which is terminated with $R_{i1}, R_{i2} = 50\Omega$ at the input. The SiGe-HBT circuit, which is currently under fabrication, consumes $30mA$ from a single $4.5V$ supply, including the $10mA$ peak current which is sourced into the VCSEL.

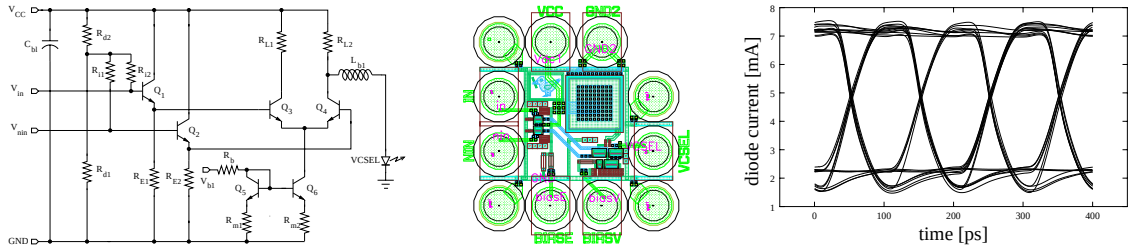

Fig. 2: Schematic (left) and layout (center) of the realized 10 Gbit/s VCSEL laser driver. The simulation using the VCSEL model developed in this work and including all bond wires shows an excellent eye opening (right).

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Gate-delay Simulations of Scaled InP/InGaAs/InP DHBTs for +100 Gb/s Applications

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InP HBT-technology is one of the most promising contenders for future high-speed ICs operating at $100\,Gb/s$ and beyond. The gate-delay τ_g, besides f_t and f_{max}, is considered one of the most important figures of merit for benchmarking digital transistor technologies. In this study, we carried out simulations of a ring oscillator (RO) to predict the influence of scaled transistor parameters on τ_g. We found that for aggressively scaled HBTs, circuit speeds in the order of $160\,Gb/s$ — which corresponds to a gate-delay below $2\,ps$ — can be obtained. We applied standard Gummel-Poon models from a commercial simulator using first-order analytical equations to incorporate the device geometry and material parameters. The device parameters were estimated and verified for a conventional triple-mesa InP/InGaAs/InP DHBT structure. A comparison between circuit simulations and first-order analytical delay expressions for τ_g showed good agreement. Our results indicate that emitter widths towards 0.25 μm are crucial for circuit speeds in excess of $100\,Gb/s$.

Introduction

InP DHBTs, though considered prime candidates for future $160\,Gb/s$ applications, still suffer from moderate scaling capability as compared to Si-technology. In this work, we investigate a scaling strategy for InP/InGaAs/InP DHBTs to achieve $160\,Gb/s$ logic speed. The high-speed performance of transistor technologies is generally described by the small-signal figures of merit f_t and f_{max}. However, the gate-delay τ_g, which can be determined roughly from the oscillation frequency of a ring oscillator (RO), is a more adequate figure of merit for logic applications. In this study we considered an eleven-stage RO with CML inverters (Fig. 1) for gate-delay simulations. The gate-delay for a single inverter stage is calculated from the number of inverters N and the oscillation frequency f_{osc} according to the formula $\tau_g = 1/2Nf_{osc}$. As a rule of thumb, we used the following approximation derived for a master-slave D-FF to relate the maximum achievable bit-rate (BR) to the gate-delay τ_g: $BR = 1/3.3\tau_g$ [1].

Scaling Simulations

A generic DHBT structure as shown in Fig. 2 was used for the simulations. We used a simplified layer structure with an InP emitter, an InGaAs base and an InP collector. The transistor parameters were calculated using simple approximation formulas as proposed e.g. in [2],[3]. The values of these formulas were included as parameters for the Gummel-Poon model of a commercial SPICE simulator. f_t and f_{max} were obtained from S-parameter simulations whereas τ_g was extracted from the voltage spectrum of the output signal of the simulated RO. By an optimization step, using a set of free parameters (e.g. the carrier velocity in the collector v_{eff}), we "calibrated" the simulated f_t and f_{max} with measured values from an existing in-house DHBT device [4]. The subsequent simulations were carried out for three different device geometries, i.e. emitter and collector widths. A constant device length $L_E = 5\,\mu m$ and a constant logic swing $\Delta V = 250\,mV$ were assumed. Vertical device dimensions were set to rather aggressive values of $W_E = 70\,nm$, $W_B = 20\,nm$ and $W_C = 150\,nm$. The choice of collector width must be considered under the aspect of low C_{BC} on the one hand and enhanced current drive capability as well as reasonable breakdown behavior on the other hand. Also thermal impacts might result from an increased current density, thus limiting the device performance. $W_C = 150\,nm$ seems to be a reasonable value to account for those effects. The base contact length S_{BS} was chosen in the order of three times the base contact transfer length. To account for the wiring delay, a π-type LC-circuit was used as proposed in [5].

Results & Conclusions

The results shown in Tab. 1 indicate that aggressively scaled emitters with S_E towards $0.25\,\mu m$ will be necessary for $160\,Gb/s$ operation. Besides a very small lateral device geometry, the need for high current densities and thin collectors will be a major issue for future scaling efforts.
A wide variety of analytical expressions for τ_g can be found for ECL and CML[1],[6],[7]. We used the analytical expression for τ_g presented in [8] for a comparison with the simulation results. For achieving bit-rates in the order of $160\,Gb/s$, a clear tendency towards small emitter widths as shown in Fig. 3 can be observed. Also, the influence of the wiring delay significantly increases for smaller emitter widths, i.e. higher bit-rates. However, using gate-delay expressions based on a summation of RC time constants yields rather conservative estimations. Therefore, the simulated data in Fig. 3 show moderate agreement with the analytical expressions.

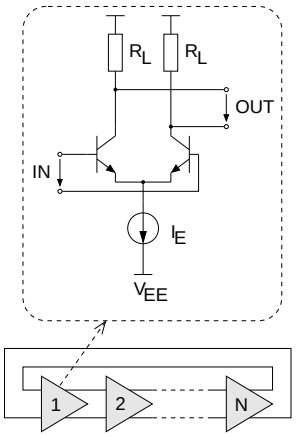

Fig. 1: N-stage RO with CML inverters.

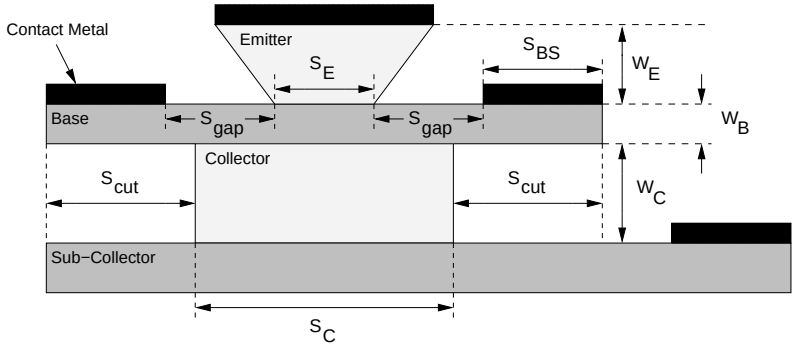

Fig. 2: Geometrical structure of the InP/InGaAs/InP DHBT used for simulations.

$\mathbf{S_E}$ $[\mu\mathbf{m}]$	**0.75**	**0.5**	**0.25**
W_E $[nm]$	70		
W_B $[nm]$	20		
W_C $[nm]$	150		
S_C $[\mu m]$	1	0.75	0.5
S_{BS} $[nm]$	300		
S_{cut} $[nm]$	375		
S_{gap} $[nm]$	200		
f_t $[GHz]$	329	331	333
f_{max} $[GHz]$	357	458	665
J_C $[kA/cm^2]$	130	170	290
τ_g $[ps]$	2.8	2.4	2
BR [Gb/s]	**108**	**126**	**151**

Tab. 1: Estimated bit-rates (BR) from three different device geometries. $L_E = 5\,\mu m$.

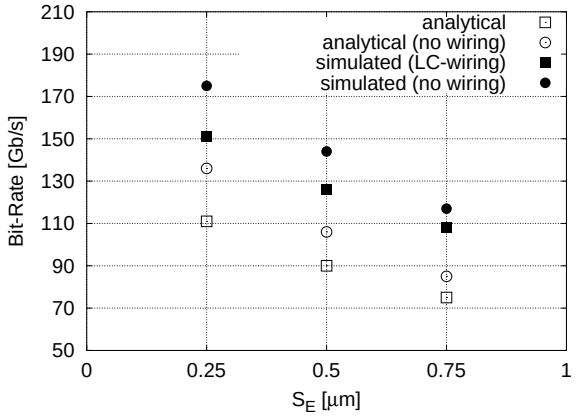

Fig. 3: Comparison between simulations and analytical expressions for τ_g. $BR = 1/3.3\tau_g$.

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Non-Reciprocal Couplers using Active Devices

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The distributed amplifier topology is adapted to form a non-reciprocal four port coupler with the objective of MMIC implementation. Simulation shows the potential performance and limitations of this device. A 2 – 20 GHz active distributed circuit coupler is demonstrated exhibiting small size, broader bandwidth and lower loss compared with standard distributed line and lumped-distributed couplers.

Introduction

The implementation of complete systems on an MMIC requires new techniques where directional couplers are needed. This is especially true for a feedforward linearizer which conventionally employs three couplers consisting of quarter wavelength transmission lines. This work demonstrates the adaptation of a distributed amplifier topology, which is readily realised in a MMIC, to form a non-reciprocal coupler.

Coupler Circuit

The distributed coupler configuration is shown in Fig. 1, where m-derived half sections are employed at the end of the gate and drain lines. Port 2 provides the coupled output and port 4 forms the through line and incorporates a buffer amplifier to improve isolation. A small signal model of a typical HEMT has been used for simulation of the circuit. It can be noted that this circuit ideally forms the input coupler of a feedforward linearizer circuit.

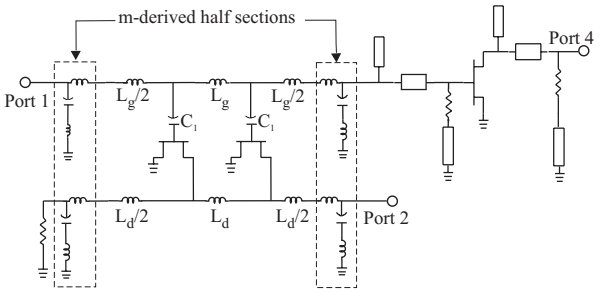

Fig. 1 Two section distributed coupler with buffer stage

A series capacitor is incorporated in the gate of each HEMT (C_1 in Fig. 1) to reduce gain to achieve the required coupling factor, 3dB or 10dB in this case. This series capacitor acts as a potential divider and reduces the voltage across each gate capacitance with a consequent reduction in gain. Computer simulation is performed for the circuit of Fig. 1 with appropriate values of C_1 to give the desired coupling factor and initially without the buffer amplifier stage. Appropriate values are substituted for the section inductances and m-derived half sections [1] to maintain $Z_0^g = Z_0^d = 50\Omega$ for both the gate and drain lines. These lumped components are then converted to microstrip transmission line equivalents for MIC and ultimately MMIC implementation. Fig.2 shows simulated responses for coupled and through ports. No optimisation has been applied, for example to reduce the ripple in the coupled port, but additional artificial line length has been added to the gate line to equalise the phase of the through and coupled lines. The simulated circuit still shows potentially useful performance especially for the 3dB coupling value. For a 10dB coupler, capacitance and inductance values become difficult to realise in practice.

The coupler isolation is governed by the reverse gain and hence the coupler will be susceptible to mismatch variations on port 4, the through port. This can be mitigated by incorporating a cascade FET on port 4 with suitable lossy matching circuitry [2] shown in Fig. 1. Greater than 20 dB improvement in isolation between port 4 and port 2 can be achieved whilst maintaining the performance of the coupler, as shown in Fig.3.

Conclusion

The distributed amplifier circuit topology has been adapted to form a non-reciprocal coupler. The potential for a two stage 3dB coupler has been demonstrated and it has been shown that use of a series capacitor on the gate to control the coupling factor yields component values which become more difficult to realize for higher coupling factors such as 10dB. Isolation is controlled by the reverse gain and can be mitigated by inclusion of a lossy match buffer stage on the through port.

Acknowledgement

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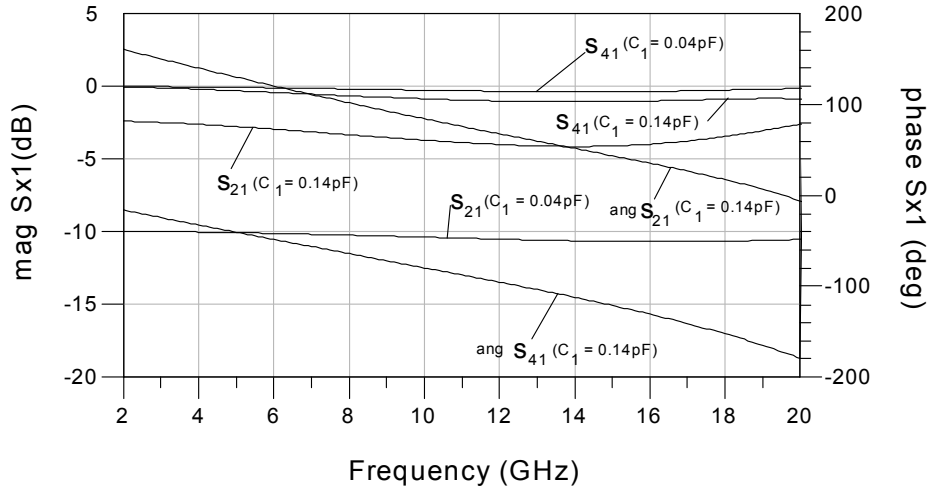

Fig. 2 Transmission and coupling factor for 3dB and 10dB couplers with two sections (n=2)

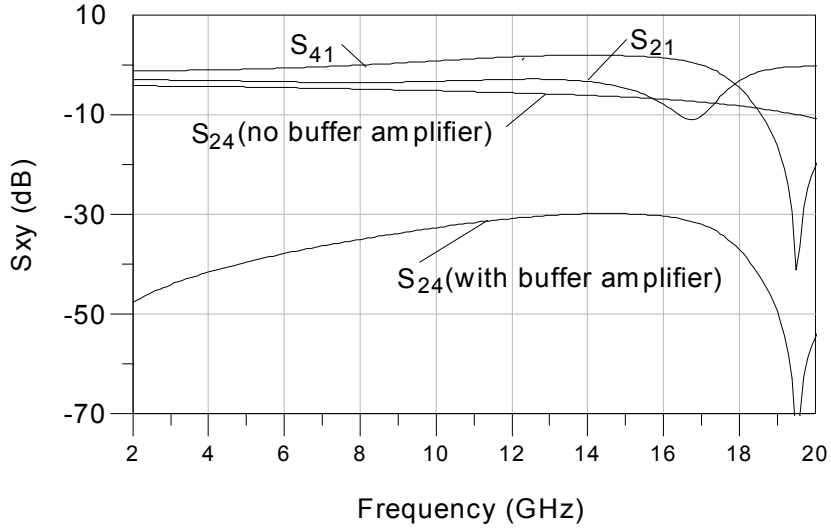

Fig. 3 Modified transmission and coupled responses after addition of buffer amplifier (n=2)

A 16-48 GHz Frequency Tripler with InP HEMTs

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***Abstract*— In this paper, we present a 16-48 GHz monolithically integrated frequency tripler fabricated with a 0.2 μm InP HEMT process using coplanar waveguide technology. The circuit is needed to generate the millimeter-wave local oscillator signal in a fiber-optic millimeter-wave radio indoor communication system. The tripler shows a peak third harmonic conversion gain of -7.3 dB and a maximum third harmonic output power of -2.5 dBm. To the authors' knowledge, this is the first double-stage InP HEMT frequency tripler ever reported.**

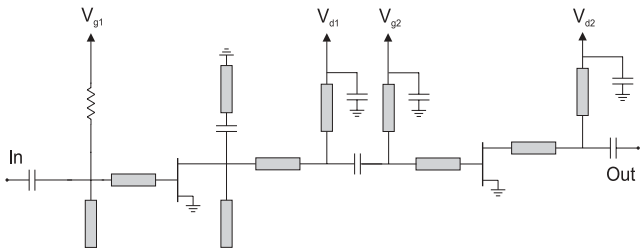

Fig. 1. Schematic of the designed double-stage frequency tripler.

I. Introduction

A very promising approach for the realization of a 60 GHz transceiver for wireless LANs is the combined use of optical-fibers and millimeter-wave radio signals [1, 2]. An important issue in the design of this kind of system is the generation of a stable high-frequency local oscillator (LO) signal in the transceiver. An efficient solution is to generate a low-frequency LO reference in the base station, to distribute it over the fiber, and to use frequency multiplication in the transceiver to generate the high-frequency LO signal. For the realization of a V-band transceiver for wireless LANs, we designed, fabricated, and characterized a frequency tripler that multiplies a 16 GHz LO signal up to 48 GHz. The used design approach will be presented in the next section. In the third section the measurements results and the performance of the fabricated circuits will be reported, while conclusions will be drawn in the last section.

II. Circuit Design

The schematic representation of the designed frequency tripler is shown in Fig. 1. The circuit is composed a frequency multiplication stage followed by a 48 GHz buffer amplifier.
For InP HEMTs, the maximum third harmonic conversion gain is obtained when the transistor is operating in class A [3]. This corresponds to the saturation region for the drain-source voltage V_{ds}, and to the peak of the transconductance g_m for the gate-source voltage V_{gs}. However, this choice results in a low conversion efficiency and leaves the designer with stability problems which are tedious to solve. For these reasons, in the design of the frequency multiplying stage, it was decided to set the device V_{gs} close to the threshold voltage V_t and V_{ds} in the saturation region. This bias point corresponds to a local maximum of the third harmonic conversion gain which ensures stability and higher conversion efficiency, but lower conversion gain.
Since at 16 GHz the input impedance of the device (2×75 μm InP HEMT) is almost purely capacitive, its input was not matched at this frequency. The network at the gate side of the HEMT solely consists in an open circuit reflector stub with an electrical length of 90^o at 48 GHz. The stub reflects the scattered power at 48 GHz back to the transistor thus increasing the conversion gain, as it has already been shown in [4] for frequency doublers. The distance between the reflector and the gate of the HEMT was optimized by means of harmonic-balance simulations. In the multiplier stage, the network at the drain side of the HEMT consists of a 16 GHz resonator which ensures the suppression of the fundamental frequency, an open circuit stub which suppresses the second harmonic, and a matching network which provides matching to 50 Ω. The biasing of the device gate is obtained through a 10 KΩ resistor directly attached to the gate line; since there is virtually no current flowing into this terminal, the voltage drop over the biasing resistor is negligible. The device drain is biased through the matching network using an on-chip RF-short capacitor.
The buffer stage is a 48 GHz amplifier with 50 Ω matching at the input and output port. Since the maximum output power of the multiplying stage does not exceed -10 dBm, the amplifier matching networks were optimized by means of small-signal simulations. A photograph of the fabricated circuit is shown in Fig. 2. The circuit was fabricated in our laboratories on a 600 μm thick semi-insulating InP substrate using a 0.2 μm InP HEMT process and coplanar wave-guide technology.

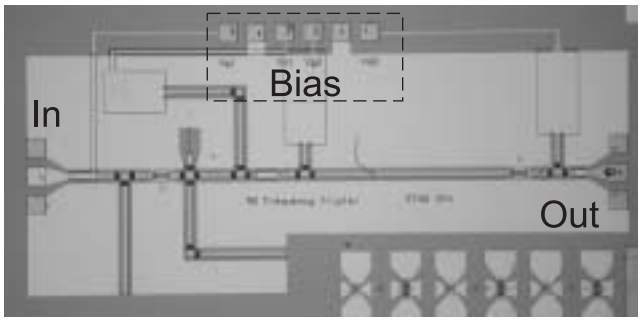

Fig. 2. Photograph of the fabricated double-stage frequency tripler. Chip size is 3.15×1.39 mm^2.

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III. Measurement Results

After fabrication, the frequency multiplication characteristics of the circuit were tested. Circuit characterization was done on-wafer using a Cascade Microtech probe station and a HP 8565E Spectrum Analyzer.

In Fig. 3, the measured third harmonic conversion gain of the double-stage tripler is presented. The peak value (-7.3 dB) is reached for an input power of 3 dBm. The multiplier stage and the 48 GHz buffer amplifier were also measured separately. From their measurement results, a third harmonic conversion gain of -3 dB was expected. The missing conversion gain can be explained assuming an inter-stage mismatch between the multiplier stage and the buffer amplifier.

The measured output power harmonics are shown in Fig. 4. The maximum output power is -2.5 dBm, reached for an input power of 3 dBm. It can be noticed that third harmonic output power does not saturate, but drops down after reaching a peak value. This is in line both with theoretical and experimental results [3]. The fundamental suppression is around 30 dB, while the power ratio between the third harmonic and the fundamental is 20 dB at the peak of the output power. The power ratio between the third and the second harmonic is around 37 dB. This is in line with the best reported results for GaAs PHEMTS [5] multipliers. The good spectral purity of the output signal is due to the combined action of the two stages. The effect of the first and second harmonic suppression network of the multiplier stage are enhanced by the filtering action performed by the 48 GHz output buffer. To the authors' knowledge, this is the first double-stage InP HEMT frequency tripler to be reported.

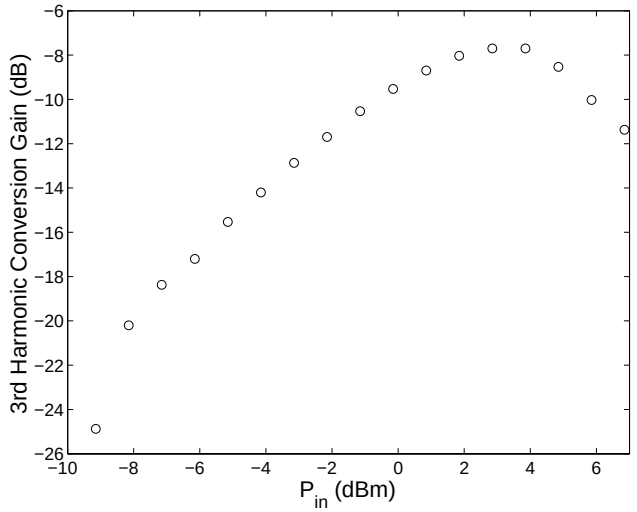

Fig. 3. Measured third harmonic conversion gain as a function of the input power for the double-stage tripler.

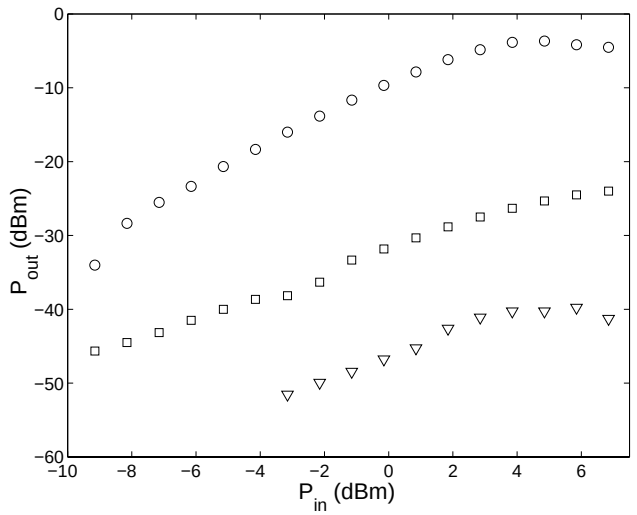

Fig. 4. Measured output power at 48 GHz (circles), at 32 GHz (triangles), and at 16 GHz (squares) as a function of the input power for the double-stage tripler.

IV. Conclusions

In this paper a double-stage 16-48 GHz frequency tripler was presented. The circuit was realized on an InP HEMT 0.2 μm process using coplanar waveguide technology. On-wafer characterization of the fabricated circuit showed a peak third harmonic conversion gain of -7.3 dB and a maximum third harmonic output power of -2.5 dBm, together with a good spectral purity of the output signal. The circuit is a suitable candidate for the generation of a stable high frequency local oscillator signal.

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VCSELs - Core Components for High Speed Optical Interconnects

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Abstract

In this paper we present the status in the development of Vertical Cavity Surface Emitting Lasers (VCSELs) that can be directly modulated above 10 Gbps. After a general introduction to VCSELs we will discuss the static and dynamic properties of VCSELs optimized for high speed modulation and applications in optical interconnects and fiber optical transceivers. We will present optimization results of the "encircled flux" parameter that extend the bandwidth-distance product in multimode fibres. The presentation will close with an overview on actual research topics and future trends.

Introduction

After more than a decade of intensive development efforts VCSELs are established as the light source of choice for short range fiber optic communication. The reason for this success is their excellent reliability, manufacturability, surface emitting geometry, symmetric beam profile and low power consumption. They are widely used in serial and parallel transceivers for Gigabit Ethernet, Storage Area Networks, proprietary system links and other applications. Key elements for a high performance VCSEL structure are an active region with high gain and excellent optical mirrors with high reflectivity and good conductivity. Commercially available VCSELs in the wavelength range of 850 nm can be modulated directly up to 3.125 Gbps. Typical applications include local area networks and storage area networks. Research and development activities focus on extending the datarates that are achieved with directly modulated devices to 10 Gbps and above.

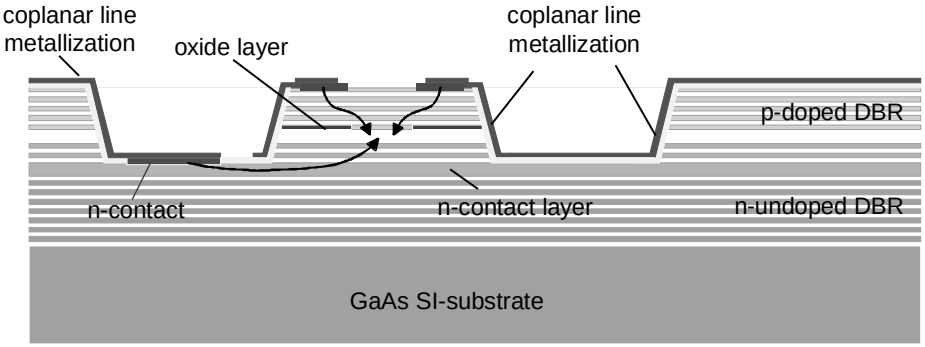

Figure 1: Cross-sectional schematic of a VCSEL structure designed for high speed operation.

Figure 1 shows schematically the layer structure of a VCSEL designed for high speed operation and datarates of 10 Gbps and above. The laser is epitaxially grown on semiinsulating substrate and both anode and cathode contacts are on top of the chip. The current confinement is provided by an oxidation layer close to the active region.

10 Gbps VCSELs

Higher datarates in optical links can be achieved by increasing the modulation speed of the individual laser and by operating several channels in parallel. Avalon Photonics is developing 10 Gbps VCSELs for serial links as well as VCSEL arrays for parallel fiberoptical transceivers with aggregate datarates ranging from 10 Gbps to 120 Gbps. As an example, figure 2 shows a picture of an Avalon Photonics 4x10 Gbps VCSEL array designed for parallel transmission of an aggregate datarate of 40 Gbps. Each indivual VCSEL channel is operated at 10 Gbps.

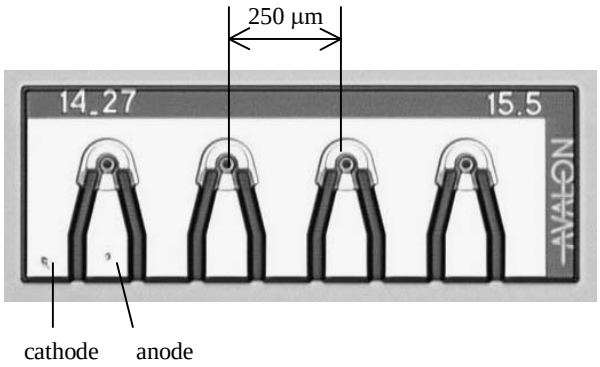

Figure 2: 4x10 Gbps VCSEL array with common cathode ground

Their top emitting geometry allows to minimize parasitics and simplifies significantly the packaging. Avalon Photonics 10 Gbps lasers have typical threshold currents of 0.8 mA, efficiencies of 0.4 W/A, and ohmic resistances of 50 Ohm. For typical operating currents of 8 mA, the output power is around 3 mW.

Measured eye diagrams of individual VCSELs modulated at 10 Gbps at an operating current of 8 mA and an operating voltage of 2 V are shown in Figure 3. Turn on and turn off times are below 40 ps, resulting in a wide open eye at 10 Gbps.

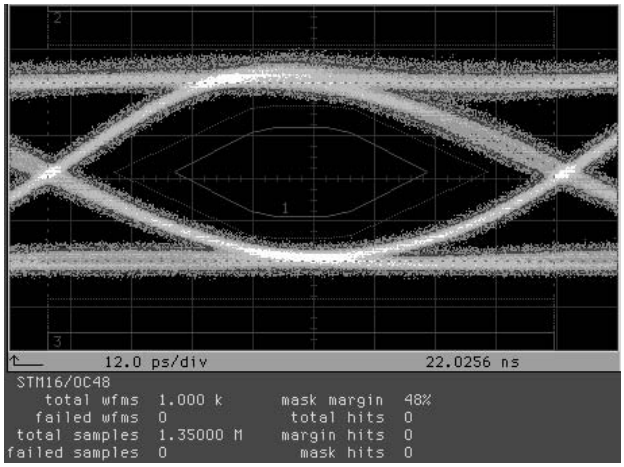

Figure 3: Measured eye diagram at 10 Gbps. The directly modulated VCSEL has a threshold current of 0.6 mA, and is biased at 8 mA. The extinction ratio is 5dB. The red lines indicate the 10 Gbps Ethernet mask according to the IEEE 802.3ae standard . The eye is wide open with a mask margin of 48%, demonstrating that Avalon Photonics VCSELs meet the stringent demands of the 10 Gigabit Ethernet standard.

Conclusion

We have shown results on directly modulated short wavelength 850 nm VCSELs that exceed 10 Gigabit Ethernet standards. These VCSELs will be used in fiberoptic datalinks in local area networks and storage area networks. Current development efforts focus on the development of high speed single mode VCSELs in the wavelength window of 1.3 and 1.5 um. This would allow to extend the applications for VCSELS to include also metropolitan networks and – ultimately – access networks.

Comprehensive Simulation of VCSELs with Applications in Industrial Device Design

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In this paper, the comprehensive 2D opto-electro-thermal simulation of vertical-cavity surface-emitting lasers (VCSELs) is demonstrated. Furthermore, device optimization with regard to higher order mode suppression in a single-mode VCSEL is presented.

Introduction

Most of today's efforts in VCSEL device design are aimed at applications in wavelength division multiplexed (WDM) optical fibre networks for data- and telecommunications. In this area, VCSEL devices offer many advantages at low cost. Technology computer aided design (TCAD) is becoming an essential tool to explore the design parameter space for an optimum solution and keeping at bay the critical cost factor, and the time required for a design cycle.

Simulation Model

The laser device model employs the photon rate equation approach. The optical fields in the VCSEL cavity are expanded into modes obtained from the complex frequency representation of the vectorial Helmholtz equation. The open nature of the VCSEL cavity is treated by employing a perfectly matched layer (PML). For the bulk thermo-electronic transport a 2D thermo-dynamic model is employed in a rotationally symmetric body. Heterojunctions are modeled using a thermionic emission model. Quantum wells are treated as scattering centres for carriers. The optical gain and absorption model in the quantum well active region is based on Fermi's Golden Rule. The subbands in the quantum well are determined by solving the stationary Schrödinger equation and a parabolic band approximation for the electrons, light and heavy holes.

Results

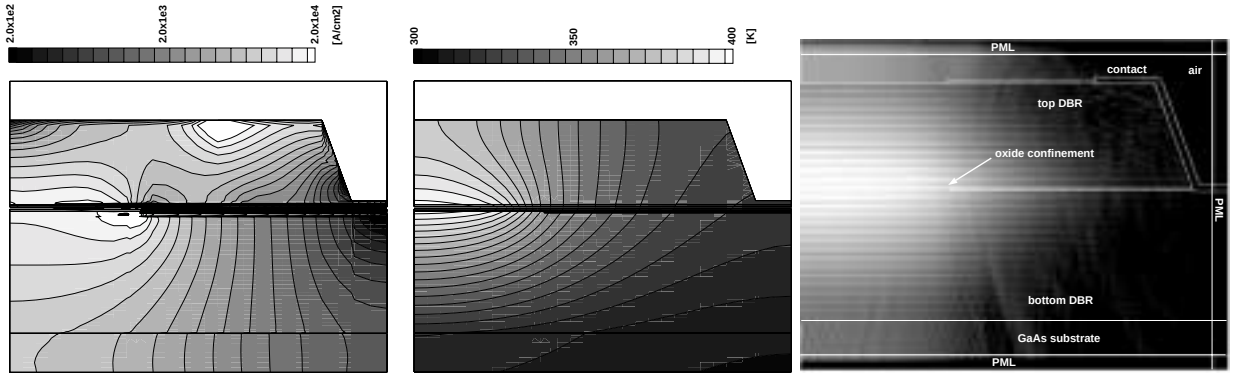

Figure 1: VCSEL simulation results. Left: current density. Center: temperature. Right: optical field.

Figure 1 illustrates the capabilities of the self-consistently coupled electro-thermo-optical simulator. The example is based on an AlGaAs(GaAs) 850 nm oxide-conned multi-quantum well VCSEL device structure presented in [1], modified to emit around 880 nm. Figure 2 shows the DC terminal characteristics as well as the spatial hole burning in the active region. The oxide cur-

rent confinement causes increased Joule heating and leads to the formation of a thermal lens at the centre of the device. This effect can only be fully accounted for if self-consistency between the optical and the electro-thermal fields is maintained. The VCSEL structure is discretised with 7729 finite elements for the electro-thermal mesh and 89'364 finite elements for the optical mesh. For computation 2.2 GBytes of memory are required.

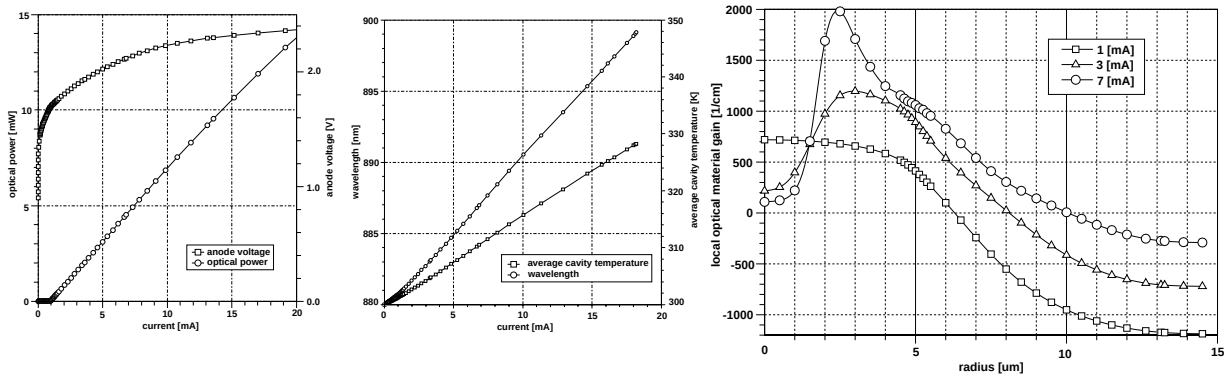

Figure 2: VCSEL simulation results. Left: DC terminal characteristics. Center: wavelength tuning of fundamental optical mode and average temperature versus terminal current. Right: local optical material gain in active region.

Conclusion

The model of a self-consistent 2D electro-thermo-optical device simulator for VCSEL devices was presented. The model is based on the photon rate equation approach. It was shown that the frequency domain FE formulation of the VCSEL optical problem can be solved efficiently and its into the context of electro-thermo-optical VCSEL simulation. The practical relevance of the implemented simulator for TCAD based design for a variety of VCSEL device structures was demonstrated with examples.

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Segmented VCSEL contact geometry for active coupling efficiency enhancement

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Active compensation of fiber misalignment from the driver side may drastically reduce the cost of VCSEL-based datacom applications by loosening their fabrication tolerances. This objective may be achieved by individually addressable segmented VCSEL contacts.

Introduction

We propose a new asymmetric drive scheme for Vertical-Cavity Surface-Emitting Lasers (VCSELs) that is expected to enable the active compensation of misalignment between laser beam and waveguide. Simulations indicate that driving the laser with two orthogonal individually addressable contacts may improve the coupling efficiency by selective excitation of modes with given azimuthal distribution. Such "electronic beam shaping" from the driver side may drastically reduce the system's costs by loosening its fabrication tolerances.

Simulations

The system-oriented VCSEL simulation tool VISTAS (*VCSEL Integrated Spatio-Temporal Advanced Simulator*) [1] [2] dynamically computes the power in each laser mode by taking into account the detailed interactions between the spatial distributions of the electromagnetic field and carriers in the cavity. It is based on two-dimensional multimode rate equations, which have been mathematically transformed (based on the physical and geometrical properties of cylindrical oxide-confined VCSELs) so as to make them better suited for numerical computations. The time required for performing a given simulation is reduced by several orders of magnitude compared to the initial formulation. Spatiotemporal intensity profiles at the laser facet can be reconstructed and transformed into far-field distributions using standard diffraction theory. Fig. 1 illustrates how such far-field profiles are employed for evaluating the butt-coupling efficiency of the beam into a waveguide [3] as a function of their relative position.

VISTAS has been employed to investigate an asymmetric drive scheme based on individually addressable segmented VCSEL contacts that is expected to enable beam shaping through preferential excitation of modes with given azimuthal distributions. Such segmented contact geometry yields azimuthal profiling of the injection current [4], and consequently inhomogeneous gain distribution. The concept is schematically presented in Fig. 2, where its influence on the far-field distribution is emphasized.

The opening of the eye diagram obtained with the asymmetric drive scheme (Fig. 3b) appears noticeably larger than in the rotational symmetric case (Fig. 3a). Various mechanisms contribute to this significant enhancement. First, reduced insertion losses resulting from the better overlap between fiber core and laser beam (see Fig. 2) explain the higher levels of both the on and off states in Fig. 3b. However, the eye diagram appears noisier in the symmetric case. This is confirmed by the relative intensity noise spectra of Fig. 4, which show a noticeably reduced overall noise level in the asymmetric case. Moreover, the low-frequency contribution to noise of mode partition [5] resulting from spatial filtering appears less marked in the asymmetric case due to the higher intensity concentrated in fewer modes [6].

The last mechanism explaining the differences between both eye diagrams of Fig. 3 is the shift of the oscillation frequency towards higher frequencies in the asymmetric case. This qualitative observation is quantitatively confirmed in Fig. 4, where a shift of more than 3GHz can be observed. Again, this is a consequence of the increased intensity concentrated in a few localized modes.

Conclusion

The highly efficient spatiotemporal VCSEL model VISTAS has been employed to investigate a new drive scheme based on two orthogonal individually addressable contacts. This technique was shown to allow

beam shaping from the driver side, and it may therefore be employed to compensate the mechanical misalignment between laser and waveguide.

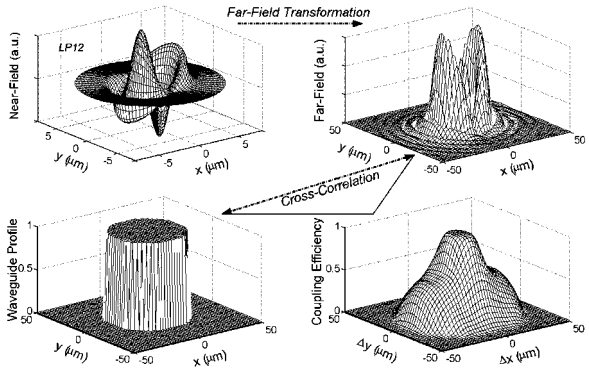

Fig. 1. Fiber coupling efficiency in misaligned cases (bottom right) computed as the cross-correlation of a 2D step-function describing the waveguide geometry (bottom left) and far-field intensity (top right) obtained by transformation of the near-field profile (top left). Note that the variables on the lower right plot are the relative misalignment components (Δx,Δy) and not the absolute position (x,y).

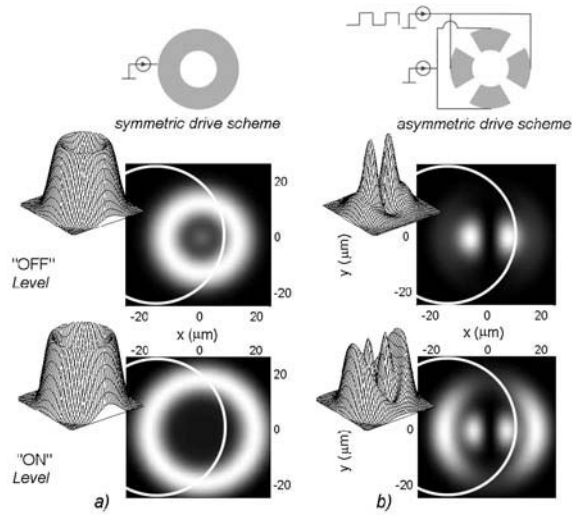

Fig. 2. Schematic description of the proposed concept for enhanced fiber coupling efficiency. The left part of the figure shows the conventional drive scheme with a ring contact and resulting degenerate doughnut-shaped far-field profiles both in the ON and OFF states. The right part of the figure shows the intensity distributions obtained with the asymmetric drive scheme. The overlap between fiber core (limited by the white circle) and far-field profiles appears clearly enhanced in the asymmetric case.

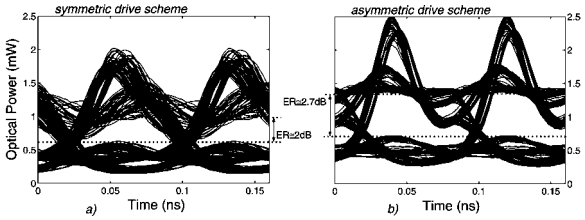

Fig. 3. Eye diagrams at 12.5Gbps obtained with the symmetric (right) and asymmetric (left) drive schemes, with a misalignment Δx=15μm between the laser beam and optical fiber.

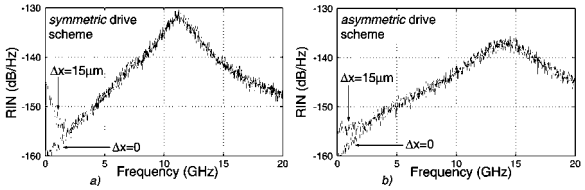

Fig. 4. RIN spectra of both drive schemes. The RIN spectra for the asymmetric case exhibit a significantly lower level over the entire range of interest (0-13GHz). Of particular importance is the drastically lower RIN level at low frequencies in the misaligned cases, which indicates reduced mode partition noise.

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Lateral index-guiding in InP-based laser diodes by oxidized AlAsSb layers

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We report on thin selectively oxidized AlAsSb layers that provide current confinement as well as optical confinement in InP-based edge emitting laser diodes. The AlAsSb layers are *p*-doped and enable an overall low series resistance of the device of 2Ω. To investigate the index-guiding of the oxidized region, far-field measurements were carried out. Good agreement between the experimental and simulated far-field patterns indicates that the partially oxidized AlAsSb layers act as a low index-cladding by the native-oxide.

Introduction

By selective wet oxidation of high Al-content compounds, current confinement and index-guiding can be simultaneously accomplished in III-V optoelectronic devices. Whereas the oxidation of AlAs is a mature technique for GaAs-based devices, the oxidation of AlAsSb is a promising candidate to adapt this technology for InP-based devices. Although AlAsSb exhibits high oxidation rates at low temperatures, upon oxidation of thick AlAsSb layers an interfacial metallic layer is formed by the segregation of Sb besides the aluminum oxide [1]. This interfacial layer causes not only a swelling of the oxidized region and, hence, a deforming of the upper cladding layers, but also, due to the metallic conductivity of Sb, it is not clear, whether the oxidized region could serve as a current aperture as well as a low index cladding in laser diodes.

As recently shown [2], thin AlGaAsSb films seem suitable to achieve homogeneous oxidation without segregation of Sb. In this paper we report on thin *p*-doped AlAsSb layers which were selectively oxidized to fulfill the demands for a current and index aperture in laser diodes.

Experimental Details

A laser structure was employed which consists of three strained InGaAs quantum wells emitting at an emission wavelength of $\lambda = 1.79\mu m$. A 25nm thick AlAsSb layer *p*-doped with Be ($p = 5 \times 10^{17}\,cm^{-3}$) was grown 100nm above the active region. After wet chemical etching of 90µm broad stripe mesas, the oxidation was carried out in a hot steam atmosphere. Due to the high selectivity of the wet oxidation process with respect to the Al-content, only the AlAsSb layers are oxidized, whereas all other layers remain unoxidized. Fig. 1 shows the schematic drawing of such an oxide-confined stripe laser. The active region is defined by the width of the remaining unoxidized AlAsSb layer. The refractive index of the oxidized AlAsSb layer is reduced to a value of about 1.6 for Al_xO_y, causing a step in the effective refractive index in the lateral direction.

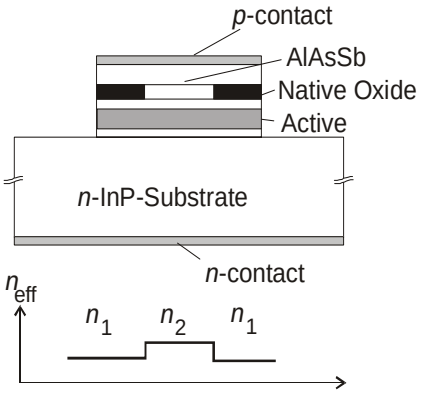

Fig.1: *Schematic cross section of a laser with an oxidized AlAsSb current aperture and the resulting effective index profile in the lateral direction*

After oxidation, lasers were cleaved and characterized by optical and scanning electron microscopy. Also the light output power-current and the voltage-current characteristics were measured and compared to unoxidized broad-area laser diodes. Furthermore, far-field measurements were carried out and compared to numerical simulations based on the transfer-matrix method.

Experimental Results

Fig. 2a shows an optical microscope image of the sample surface after oxidation at 360°C for 10 minutes. In this laser structure, a 25nm thick AlAsSb oxidation layer is embedded between two InAlAs layers. As can be clearly seen, the surface is smooth and shows no deformations. The oxidation depth is uniform and isotrope for the (110) and (-110) directions. Also scanning electron microscope images of the cross section of the oxide show no interfacial layer around the native oxide (c.f. Fig. 2b).

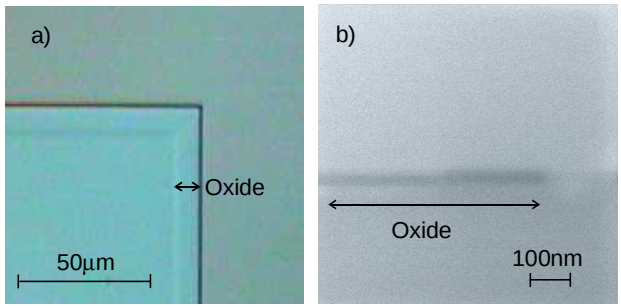

Fig. 2: *a) Optical microscope image of the surface and b) cross sectional SEM image of the InAlAs/AlAsSb/InAlAs stack after partial lateral oxidation*

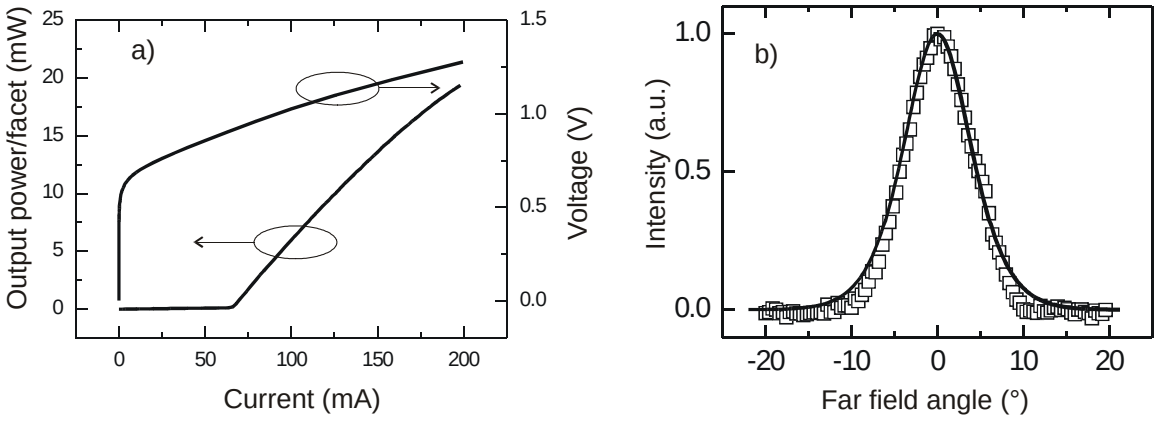

Fig. 3: *a) CW output power-current characteristic of a 1mm long laser with 5µm current aperture at 20°C; b) measured (squares) and simulated (line) horizontal far-field pattern*

Fig. 3a shows a typical continuous-wave (CW) output power-current characteristic of an oxide-confined laser at 20°C. The laser has a cavity length of 1mm and a current aperture of 5µm. The lasing threshold is reached at a current of 66mA. Taking current spreading by carrier diffusion into account, this corresponds to a threshold current density of 940A/cm². Due to the broad *p*-contact area the laser shows a series resistance of only 2Ω. The value of the external differential quantum efficiency is about 60% indicating that only low optical losses are present. The far-field pattern at a current of 100mA is depicted in Fig. 3b. The measured full-width at half-maximum (FWHM) angle is about 9.5°. An index step of 0.004 in the lateral direction was found by simulation of the far-field patterns.

Conclusion

We have demonstrated the capability of thin oxidized AlAsSb layers for achieving lateral index-guiding in edge emitting lasers on InP substrates. Besides providing index guiding, the oxidized AlAsSb layers also act as an electrical insulator and give excellent current confinement. Our results encourage the development of vertical-cavity surface-emitting laser diodes that employ native-oxide AlAsSb layers for the current confinement and index-guiding.

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High-power laser diodes with improved beam quality

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A dry-etching process for laser fabrication with vertical, smooth, and flat facets was developed. Using this optimized chemically assisted ion-beam etching (CAIBE) process, unstable-resonator lasers were fabricated and investigated. Such a device exhibits an optical output power of 1.6 W. Virtual source sizes are in the range of 5 μm (FWHM) with more than 80 % of the intensity in the single main lobe for all tested powers. The brightness of such laser devices is about one order of magnitude higher than the brightness of broad-area lasers and therefore suitable for high-efficiency fiber coupling.

Introduction

The brightness of narrow-stripe laser diodes is usually limited by catastrophic optical mirror damage (COMD). Although increasing the width of the apperture increases the output power, the brigtness of broad-area lasers is poor. One possibility to overcome this barrier is the use of unstable-resonator semiconductor lasers with dry-etched curved mirror facets. The output mirror apertures can be increased leading to higher powers compared to narrow-stripe lasers. together with an improved brightness compared to broad-area lasers [1].

Epitaxy

The epitaxial layer sequence of the lasers is a MBE-grown graded-index separate-confinement heterostructure (GRINSCH) [2]. The active region consists of an single 8-nm-thick compressively strained $In_{0.2}Ga_{0.8}As$ quantum well which is surrounded by 10-nm-thick GaAs spacing layers followed by doped AlGaAs grading and cladding layers. The p- and n-dopants are C and Si, respectively. The emission wavelength of the laser devices is 980 nm.

Fabrication

The fabrication of unstable-resonator lasers is basically the same as for broad-area lasers. However, the curved mirrors are fabricated with an optimized chemically-assisted ion-beam-etching (CAIBE) process and a 3-level resist as etch mask [3, 4]. The dry-etched mirrors require vertical, flat, and smooth facets. AFM measurements show a remaining roughness of 3–5 nm (RMS). AR/HR coated devices were mounted junction-side down on diamond heatspreaders. Figure 1 shows the the dry-etched curved rear facet of an unstable-resonator laser diode.

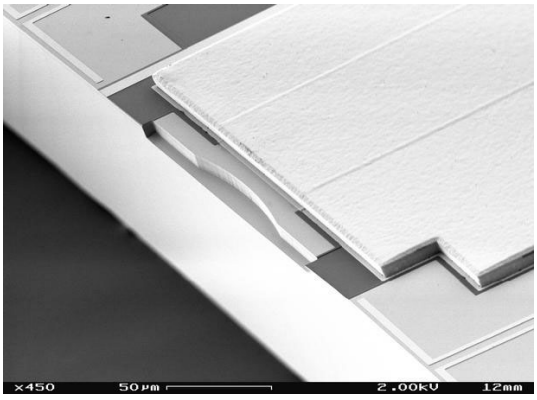

Figure 1: SEM picture of the dry-etched curved rear facet of an unstable-resonator laser diode.

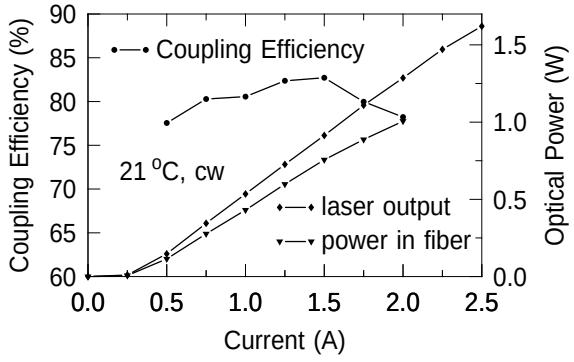

Figure 2: Output characteristics of an unstable-resonator laser coupled into a 25 μm fiber.

Characterization

All measurements were performed under cw operation at room temperature. The L–I curves of unstable resonators show slightly decreased efficiencies compared to broad-area lasers, due to the losses of magnification. Differential quantum efficiencies of 60 % and threshold current densities of 225 A/cm^2 were achieved for a 1000 μm resonator with 500 μm back-side-mirror curvature radius and 200 μm output apperture. The output power at 2.5 A is 1.6 W and is not limited by roll over or COMD. From the measured corrected far field patterns, the size of the virtual source can be calculated to be in the range of 5 and 15 μm at FWHM and 1/e^2, respectively. These values stay almost constant for all pump currents. The position of the virtual source is in the range of 340 μm and remains also stable for all pump currents. The shape of the corrected far fields are almost single lobed with about 80 % of the output power in the main lobe. First simple fiber-coupling experiments into single-mode fibre show coupling efficiencies of up to 25 %. However, coupling into a 25 mum fiber leads to powers of over 1 W, which is shown in Fig. 2.

Conclusion

For unstable-resonator laser fabrication, a dry-etching process was developed leading to vertical, smooth, and flat facets. With this optimized etching process, unstable-resonator lasers were fabricated and characterized. An optical output power of 1.3 W at 2 A pump current without thermal roll over or COMD was achieved. A differential quantum efficiency of 60 % and a threshold current density of 225 A/cm^2 were measured. The virtual source sizes are 5 and 15 μm at FWHM and 1/e^2, respectively. The position of the virtual source inside the laser is located in the range of 340–345 μm behind the output facet and almost independent of the pump current. More than 80 % of the intensity of the virtual source is included in the main lobe. The brightness of such laser devices is about one order of magnitude higher than the brighness of broad-area lasers.

Acknowledgments

We are grateful to Roland Jäger, who grew the epitaxial material. The AR/HR facet coating was performed by Franz Eberhard, OSRAM Opto Semiconductors, Regensburg, Germany. This work was supported by the IST Programme of the European Commission as part of the WILD Project IST-1999-10787 and by the German Federal Ministry of Education, Science, Research and Technology (BMBF) under contract 13N7827.

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Hybridization technology for extended-wavelength InGaAs-on-GaAs Detector Arrays

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We developed an electro-plating process to deposit Indium on detector array substrates. The process has been demonstrated on fully processed 3inch extended-wavelength InGaAs-on-GaAs detector array substrates with high yield. We believe that the plating process can be used for the integration of a full range of detector or other substrates.

Introduction

Sensing in the short-wave infrared (SWIR) necessitates various types of detector arrays depending on the particular application. Detector arrays range from large pitch linear arrays to very dense 2D focal-plane arrays. In particular during recent years there has been increased interest in extended spectral cut-offs up to about 2.5µm. Detector materials are InGaAs and Mercury-Cadmium-Telluride (MCT). It is well know that both material systems suffer from difficult growth due to lattice mismatch & usually require sensitive substrates. As a result, detector layers tend to be inhomogeneous across the substrate. The processing of detector arrays on such layers before hybridization has been optimized in recent years and allows virtually the transfer of the bare layer quality to the detector arrays with moderate to high yield. At this late stage the detector array needs to be integrated with the read-out IC (ROIC) and therefore a high yield bonding process is required. There are two major bonding techniques: wire bonding and solder bump flip-chip processes. Wire bonding is only viable for linear arrays and not too small a bond pitch (currently around 60µm), thus limiting the number of pixel. Since small pitch & large detector count are typical for SWIR sensors the favorable technique is flip-chip. The actual flip-chip process is chiefly a single die process, however, bumping (i.e. the deposition of the solder bump) can be done on a full substrate or on a single die. The bumping can be on the detector substrate, the ROIC or both. The interconnect material of choice is Indium since it keeps its plasticity down to low temperatures and can therefore accommodate the mismatch of thermal expansion between ROIC & detector array during cooling. There are two major deposition techniques: evaporation & electrolytic deposition (plating). The required metal thickness is large (~5µm). Evaporation is slow & wastes large amounts of Indium. Patterning of the thick metal (e.g. by lift-off) with large yield is difficult. This technique is, however, substrate independent. Plating sets restrictions on the substrate (e.g. contact metals) and it requires substantially more process development. Yet, the material consumption is limited and Indium is only deposited where needed. This feature makes it very promising for detector array hybridization.

Experiment

Homojunction n-on-p 78%-InGaAs photodiodes were grown on 3” semi-insulating GaAs by means of molecular beam epitaxy. Since the difference of the lattice constants of InGaAs and GaAs is about 7% the active layer of the diode was grown on top of a transparent buffer (InAlAs). The detector is, thus, suitable for backside illumination. A 3inch wafer was processed using standard microelectronics manufacturing technologies (photo-lithography, etching, planarization, metalization) to produce 31dies of 2-dimensional arrays of single detectors. Key dimensions of the detector array were as follows: 256x320 pixels, 30µm pitch, a fill factor of about 64% & a detectivity of D^*~$7 \cdot 10^{10} Hz^{1/2}$cm/W @ 250K & 1.6µm.

After the array process a sacrificial layer (TiW) was deposited and openings of the thick resist (AZ4562) were defined by contact lithography. Then, Indium was plated on the wafer in a solution of $InCl_3$ at a controlled potential to reduce hydrogen formation. A fully

processed and plated wafer is shown in Figure 1. After the plating there was a thermal reflow and the sacrificial layer was removed.

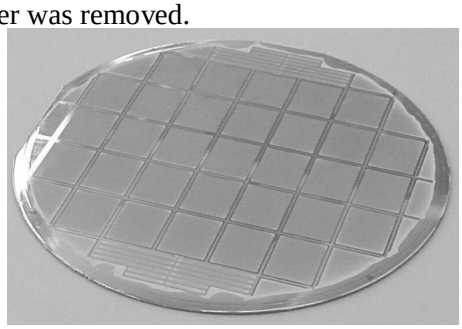

Figure 1 Fully processed and plated 3inch GaAs wafer with 31 detector

An array was then singled out from the wafer and hybridized to a commercial ROIC from Indigo Systems™. After flip-chip processing, the die was packaged using a custom package with an integrated 2-stage thermo-electric cooler. The package was then sealed in a dry and inert atmosphere to prevent sensor degradation and icing. For testing purposes the sensor was mounted on a test PCB on an air-cooled heat sink. The required timing of the read-out circuit was provided using a FLEX10K20 FPGA board and the buffered output was sent to the analogue input of a frame grabber (Matrox Pulsar) with an 8bit resolution. The system is connected to a PC where raw and corrected frame data is presented in a LabVIEW environment. During testing the sensor was cooled to 250K.

Results

On wafer scale we observed a considerable gradient in plating thickness related to the sheet resistance of the sacrificial layer. The amount of deposited Indium varies by almost a factor of two between the edge and the centre of the wafer. This is, however, no obstacle for the hybridisation since plating showed to have good uniformity across a single die. The plating yields were >99.8 for 7 of 31 & >98% for 25 of 31 dies (counting the number of missing bumps & defects). We took a macro-image of a SWIR LED (emitting at 1.9µm) to demonstrate the functionality of the sensor.

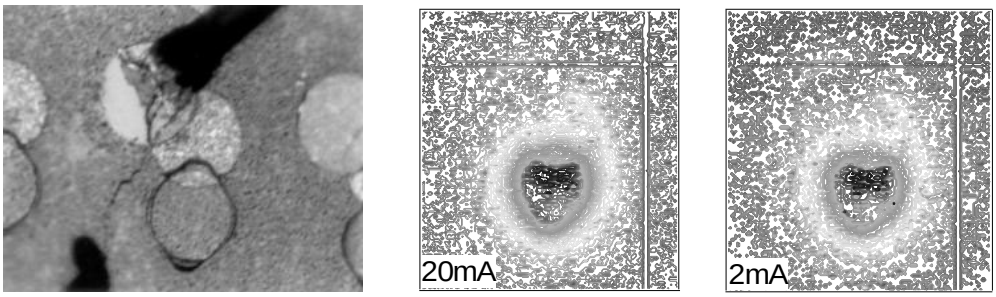

Figure 2 Images of a 1.9µm LED at the left in the visible range and at the right in the SWIR at two different driving currents showing evidence of current crowding

Conclusions

We have demonstrated the feasibility of a high yield Indium plating process, which allows the flip-chip integration of high density 2D detector arrays. A similar process has been used for linear array sensors with 256pixel on 25µm pitch on 2inch substrates. We therefore believe the technology to be viable for a range of substrates sizes and substrate types.

A Fokker-Planck model for impact ionization and carrier multiplication in avalanche photodiodes

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A high field transport model for impact ionization based on a Fokker-Planck Equation (FPE) is presented. Two results are reported in this paper. (1) a new analytical expression for ionization coefficient that is valid at high electric fields and (2) a novel scheme to compute bipolar carrier multiplication in sub-micron avalanche photodiodes (APDs). The computed results show excellent agreement with the results of Monte Carlo simulations in both cases.

1 Introduction

In APDs with sub-micron multiplication region widths, the internal electric field can exceed a few hundreds of kV/cm, at which the nonlocal aspects of impact ionization become significant. Conventional carrier transport models are inadequate in this situation and usually one has to resort to computationally expensive Monte Carlo (MC) methods. Recently, however, an alternative model based on FPE has been shown to be very accurate and economical in describing both the steady state [1] as well as transient behaviour [2] of nonlocal impact ionization. The next section briefly describes two results that have been obtained from an analysis based on FPE. A parabolic energy band model with only momentum randomizing optical phonon scattering has been assumed for both cases.

2 Results and Discussion

(1) *A new analytical model for ionization coefficient*: The most important quantity that is used to characterize impact ionization is the ionization coefficient, conventionally defined as the probability per unit distance along the direction of the field for a carrier to impact ionize. The major aim for any ionization model is to determine how the ionization coefficient varies with electric field. A new expression for the ionisation coefficient, α, valid at high fields has been derived from an analytical solution of the steady state FPE. Figure 1 shows the good agreement between normalized ionization coefficient computed using this expression with the ionization coefficients predicted by MC simulation (triangles) for two different values of hard threshold energy, $E_{T.}$

(2) *A novel method for bipolar carrier multiplication simulation*: Any model that attempts to calculate the time evolving avalanche carrier concentration in APDs must consider the following three major tasks: (i) *to describe the evolving carrier distribution at high electric field,* (ii) *to describe the ionization events in space and time and finally* (iii) *to incorporate the freshly generated carriers*. The success of FPE for the first two tasks has been discussed elsewhere [3, 2]. In this work the FPE has been extended to incorporate the secondary electron-hole pairs. Thus a complete simulation of the time-dependent evolution of the coupled bipolar carrier multiplication has been performed for the first time within the FPE framework. Compared to MC simulation, this new approach is considerably faster and is suitable for implementation in conventional device simulators. In the problem considered here, the time dependent electron and hole distributions in an avalanche region of width, w = 0.1 μm, under an electric field, F = 762 kV/cm, due to an electron injected at x = 0 at t = 0 (equivalent to a Dirac delta function initial condition for the electron concentration) has been computed. Figure 2 shows the excellent agreement between the FPE results (lines) and the MC simulation (symbols) for the electron concentration at four different times (0.1 ps (circles), 0.2 ps (triangles), 0.4 ps (squares) and 0.8 ps (diamonds)). At t = 0.1 ps the electron concentration consists mainly of the primary (injected) carriers since the impact ionization has not yet begun. However at 0.2 ps, the presence of secondary carriers (the hump at ~ 0.05 μm) is clearly evident. Without any adjustable parameters, the FPE model reproduces the MC result for the carrier concentrations, except at later times (0.8 ps) when the FPE concentration has been found to decay away faster than the MC one.

3 Conclusions

For the steady state case an analytical solution for the space and energy dependent carrier distribution has been obtained from which a new expression for ionization coefficient has been derived which

agrees with MC prediction. As an extension of the FPE model, a novel method to compute the bipolar carrier concentration in a simple APD structure has also been presented.

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5 Figures

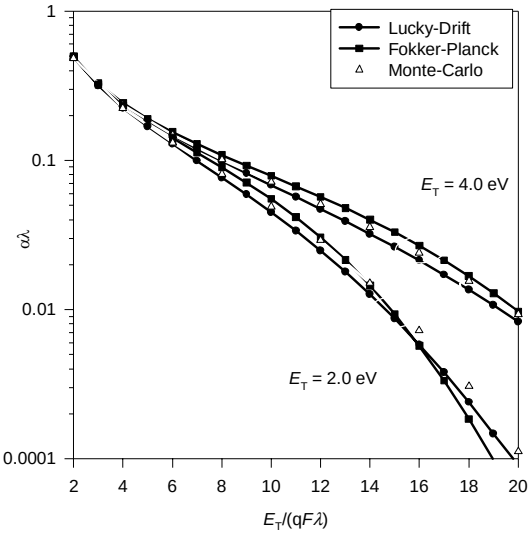

Figure 1: Normalized (λ is the momentum mean free path) ionization coefficient computed from FPE (squares) and MC (triangles) for two different values of hard threshold energy, E_T. The lucky drift prediction (filled symbols) is also shown.

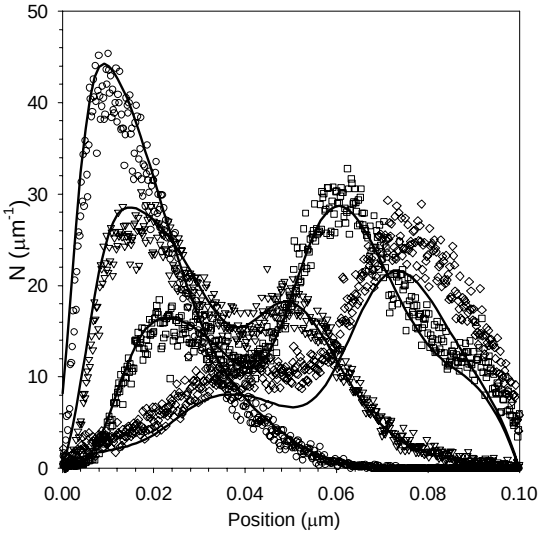

Figure 2: *Electron concentrations* (*lines*) *for a 0.1 μm depletion region width thick p-i-n structure at F = 762 kV/cm at four different times* (*0.1 ps* (*circles*), *0.2 ps* (*triangles*), *0.4 ps* (*squares*) *and 0.8 ps* (*diamonds*)) *computed using the bipolar FPE equation. The symbols represent the results from an equivalent bipolar MC simulation.*

Bi-dimensional photonic crystals: from basic crystals to optical device applications

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Photonic crystals (PhCs) are fundamental tools to study and control light propagation on the wavelength scale. In particular, the potential of bi-dimensional PhCs for miniature integrated optics circuits is a topic under intense investigation. In this paper we discuss bi-dimensional PhCs exhibiting clear photonic band gap effects which were fabricated in GaAs- and InP-based heterostructures. An internal light source technique was used to characterize their optical performances. A phenomenological model was developed to study out-of-plane radiation losses. Finally we comment on several types of photonic crystal structures for device applications which were theoretically and experimentally investigated.

Introduction

Photonic crystals (PhCs) consist of periodic arrangements of dielectric (or metallic) elements with a strong dielectric contrast [1]. In these structures the achieved wavelength-scale periodicity affects the properties of photons in a way similar to that in which atoms in semiconductor crystals affect the properties of electrons. Thus, light propagation along particular directions is forbidden within relatively large energy bands known as *photonic bandgaps* in analogy with the concept of electronic bandgap in semiconductors. Initially proposed as a generalization of one-dimensional (1D) dielectric Bragg mirrors to two or three directions [2], PhCs have opened new ways to tailor the light-matter interaction and in particular to control spontaneous emission. Moreover the introduction of line or point defects into simple PhCs results in allowed photonic states inside the bandgap. The properties of these allowed states are dictated by the nature of the defect, *e.g.* guided modes propagating in a line defect [3] or cavity modes confined in a point defect [4]. These promising characteristics of PhCs have led to the design of new photonic systems with potentially superior properties for photon confinement [5-6].

Three-dimensional (3D) PhCs are, from the basic point of view, the ideal material for light control. Nevertheless, their fabrication is still a large challenge and many techniques are being investigated in order to achieve 3D semiconductor-based structures both at optical and at infrared wavelengths [5-6]. Reproducibility, reliability, control of PhC parameters, application to real devices, etc., however remain open issues.

On the other hand, it has been proven that a bi-dimensional (2D) PhC combined with a step-index waveguide in the vertical direction (see Fig. 1) offers enough light control for integrated optics applications [5-7]. The potential of this approach has been successfully demonstrated both in GaAs-based [7] and in InP-based [8] structures. With respect to the fabrication of 3D PhCs, remarkable advantages stem from the use of mature fabrication technologies, such as standard epitaxy, electronic beam and dry etching lithography techniques.

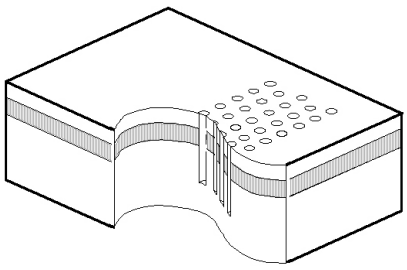


Fig. 1: Sketch of a bi-dimensional PhC in a waveguide geometry

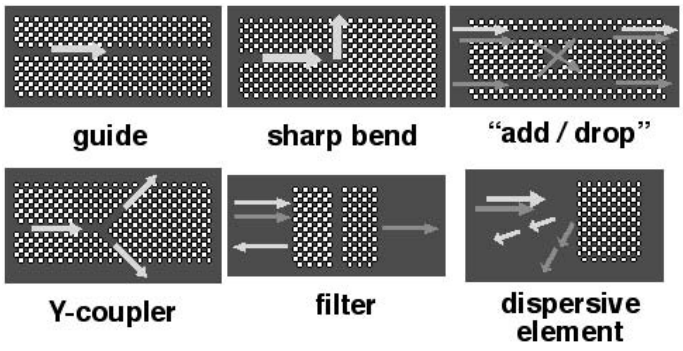
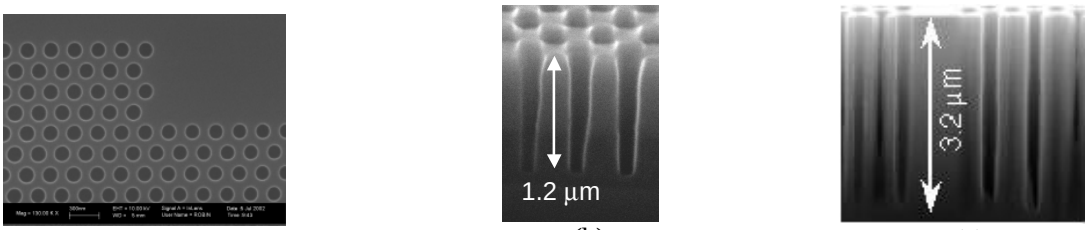


Fig. 2: Examples of PhC-based integrated optics building blocks and complex functions.

In the last few years, the possibility of exploiting the novel capabilities of 2D PhCs for photonic integrated circuits has been envisaged [9] and the use of 2D PhCs is being widely explored in order to improve the performances of integrated optics devices [10]. Some basic functions of integrated optics (*i.e.* bends, filters, splitters, etc.) are depicted in Fig. 2 together with more complex functions based on guides coupled to resonators [6,11] or on the use of the dispersive properties of PhCs [12]. Furthermore, the possibility of embedding an active region in the vertical guiding structure of *quasi*-2D PhCs allows the development of hybrid active/passive building blocks [13].

Basic 2D PhC structures: fabrication and optical characterization

In order to fulfil the expectations of novel and greatly improved devices, suitable PhCs for optical wavelengths need to be fabricated with high precision. Up to now different solutions based on standard semiconductor technology have been developed according to the base material system in use, *e.g.* GaAs-based or InP-based heterostructures. In the first case, our approach consisted of etching deep air holes into an epitaxially grown GaAs/AlGaA*s* waveguide [Fig. 3 (a)-(b)]. Electron beam lithography was used to imprint the PhC structure in a PMMA mask. Pattern transfer from the « soft » PMMA into the « hard » semiconductor required an intermediate layer of SiO_2. Reactive ion etching (RIE) based on fluorine chemistry (CF_4/H_2) was used to etch this intermediate layer. Finally the pattern was transferred into the semiconductor by means of RIE based on chlorine chemistry ($SiCl_4$) with a fraction of O_2 added into the chamber. The addition of O_2 leads to the formation of a thin oxide layer on the sidewalls which improves the verticality of the etched features.



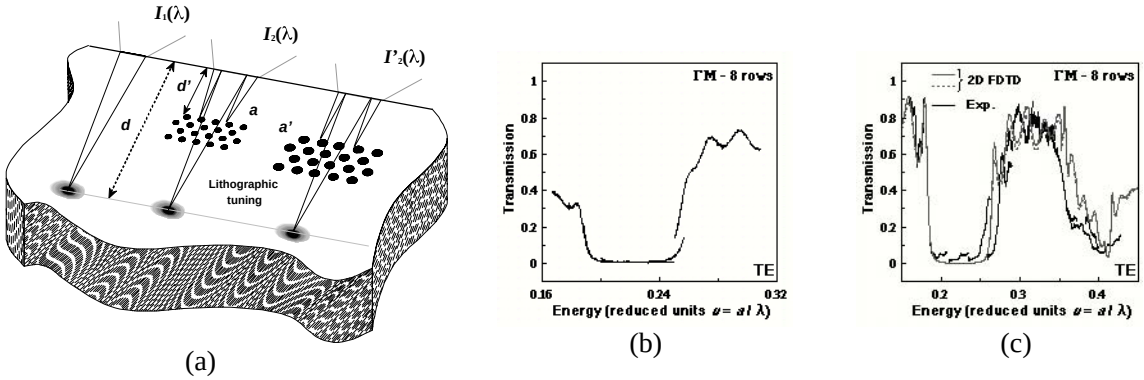
(a) (b) (c)

Fig. 3: (a) SEM top-view of a PhC with a 240 nm period; lateral view of a PhC after mask tranfer into (b) GaAs- and (c) InP-based heterostructures by RIE and ICP etching, respectively.

As for InP-based PhCs, several fabrication techniques were investigated in the framework of the IST-PCIC project [10]. The same three-step procedure described above was adopted and three etching techniques proved to be suitable for an optimized pattern transfer into the semiconductor heterostructure: electron cyclotron resonance-reactive ion etching (ECR-RIE) [8], chemically assisted ion beam etching (CAIBE) [8] and inductively coupled plasma etching (ICP) [Fig. 3 (c)] [14].

In order to investigate the optical properties of the etched PhC structures we set up an internal light source (ILS) technique [see Fig. 4(a)] [8]. In the last few years, this technique has been successfully applied to the study of 2D PhCs deeply etched in semiconductor step-index waveguides [6-8]. This method has been demonstrated to be a powerful tool in assessing fundamental PhC properties and in measuring reflection, transmission, and diffraction. It has also been shown to eliminate some of the difficulties and uncertainties arising in standard optical techniques (*e.g.* the end-fire method) [7-8].

We used the ILS technique to measure transmission spectra through 2D PhCs consisting of a triangular lattice of air holes etched through a monomode waveguide. Different emitters (*e.g.* quantum wells or quantum dots) were embedded in the core layer so that photoluminescence (PL) emission can be excited and used as a built-in probe beam. Part of the PL signal propagates parallel to the surface as a guided mode and interacts with the PhC structure before it escapes from the cleaved edge where the light is collected. From this, the absolute PhC transmission is obtained by normalizing this spectrum with respect to a spectrum collected from a non-patterned region of the sample. For example, transmission spectra were measured through simple PhC slabs along both ΓM and ΓK lattice orientations. For GaAs-based structures the transmission through 8-row thick slabs is suppressed down to 0.2% inside the gap and increases up to 70% outside [see Fig. 4(b)]. For InP-based PhCs well-defined photonic bandgaps appear in all spectra, while transmission values up to 80% are found in the *dielectric* (low energy) and *air* (high energy) transmission bands [see Fig. 4(c)].



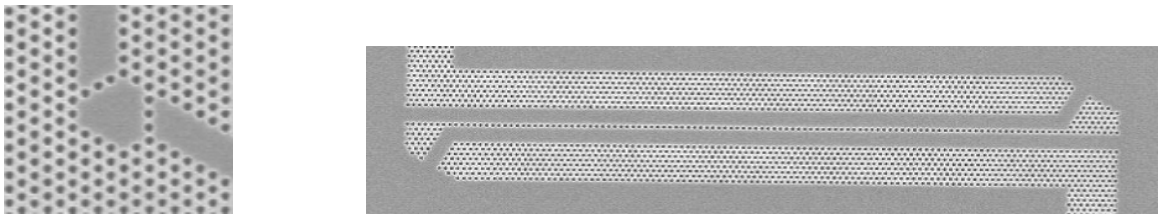
(a) (b) (c)

Fig. 4: (a) Internal light source technique for optical characterization of PhC structures; trasmission spectra through 8-row thick ΓM *PhC slabs etched in (b) GaAs- and (c) InP-based heterostructures by RIE and ICP etching, respectively. In (c) calculated spectra (gray lines) are reported for comparison.*

It should be noted that the transmission level out of the photonic bandgap is affected by out-of-plane losses in the PhC. Therefore, from the analysis of the transmission bands information can be obtained on the quality of the PhCs. In particular, we developed a phenomenological analysis of radiation losses in planar PhCs induced by the finite hole depth and the cylindro-conical hole shape. An imaginary dielectric constant was added in the air holes to account for out-of-plane scattering. The latter constant was decomposed into an intrinsic loss term (ε''_{int}) and a hole shape factor (ε''_{hole}) [15]. Three different hole-shapes were considered : (*i*) cylindrical holes of finite depth, (*ii*) conical holes in the bottom cladding [15], and (*iii*) truncated-cone holes [16]. Establishing a figure of merit for losses generated by cylindro-conical holes, allowed us to identify different regimes where depth and sidewall verticality affect the PhC optical properties to a different extent. This model proved to be a powerful tool avoiding the task of heavy 3D calculations in the design of many PhC applications. The combination of theoretical and experimental results led to a thorough investigation of the hole shape contributions to out-of-plane losses. Clear perspectives were identified for the fabrication process, while optical measurements were used to check and validate the progress of the etching techniques.

Passive PhC-based structures for device applications

The advantage of 2D PhCs for miniature photonic integrated circuits lies in the possibility to integrate different functionalities on the same optical chip. In order to connect different building blocks (*e.g.* filters, combiners, etc.) a PhC-based structure is needed. Channel waveguides designed in PhCs and operated at frequencies within the bandgap are expected to provide guiding with low losses [17] and to allow sharp bends [6]. The quantitative evaluation of propagation losses in straight channels [18] and the development of optimised bend designs [6] are topics under intense investigation. However, the combination of the small bandwidth and the best reported loss levels (*e.g.* 6-10 dB/mm for straight guides [6,18] and –1.1 to -3 dB/bend [6,19]) is still an obstacle for dense integration.



(a) (b)

Fig. 5: SEM top-view of (a) an asymmetric resonant cavity bend and (b) a linear waveguide coupler.

We designed bend structures where asymmetric cavities are used to couple two straight waveguides [Fig. 5(a)]. With respect to more standard bend designs [6,19] inserting a cavity in the waveguide path opens the way to numerous applications (*e.g.* axial filter devices). Moreover, the advantage of using asymmetric cavities instead of standard hexagonal cavities [6] stem from the

presence of non-degenerated modes in the asymmetric cavity. These structures were patterned in GaAs-based heterostructures and transmission measurements were performed. An improved bandwidth was found with respect to more standard designs, but to the expense of the transmission level.

Another important functionality in integrated optics is the coupling of light between parallel waveguides. This can be achieved by means of linear PhC waveguide couplers. We investigated basic co-directional couplers where the key parameter is the coupling length (L0), *i.e.* the distance after which the light has completely switched from guide A to guide B. Real structures were fabricated in GaAs-based heterostructures and transmission measurements were performed. The experimental L0 value was found to be 275 rows, *i.e.* in the domain 40 to 70 μm. These lengths are well above the wavelength scale, but they are much less than the size of classical integrated optics structures, thus allowing higher device density.

Finally, an important step towards the application of PhC structures in optical devices is the possibility of finely adjusting PhC properties, *e.g.* by means of temperature tuning. Using the experimental method described in Ref. [20], we measured the modes of hexagonal cavities in 2D PhCs as a function of temperature. We obtained a wavelength shift of about 5 nm for a temperature difference of about 56°C which could be used for thermo-optical tuning of basic PhC components at a lab level. Nevertheless, this solution is limited by the high thermal conductivity in III-V semiconductor materials and such effects will have to be considered and compensated for real PhC applications.

Conclusion

In this paper we presented an overview on progress in PhCs from fundamentals to device applications. We believe that three ways can be foreseen in which PhC concepts will have a major impact in the field of photonic integrated circuits:
(*i*) they allow the fabrication of high performance optical devices with very small sizes;
(*ii*) they can be made through highly-simplified and low-cost fabrication routes;
(*iii*) they allow novel functions due to their special physical properties or diffraction effects.

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Deep dry etching of InP with a $Cl_2/CH_4/H_2$ mixture on an ICP-RIE for photonic crystals.

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Photonic crystals (PhC) allow the control of light over dimensions of the order of the wavelength. We fabricate planar PhCs including a conventional slab waveguide in the vertical direction. For telecommunication wavelengths, the InP material system is used, and ultra-small and deep holes are required due to the low refractive-index contrast of the lattice-matched quaternary compounds. Therefore an etching technology with a high selectivity against the lithographic mask and high aspect-ratio up to 1:10 is needed. In this paper, we present our PhC fabrication technology using an inductively-coupled plasma (ICP) reactive-ion etching (RIE) system. We give a short overview of the mask fabrication and then discuss the impact of different parameters on hole quality and etch depth evaluated with the aid of the design of experiments (DOE) method of G. Taguchi.

I. Introduction

PhCs are structures with a periodic modulation of the refractive index, e.g., fabricated by etching holes in the order of the wavelength into a semiconductor material. These structures have interesting properties for molding the flow of light [1] in the sub-micron regime. The periodic modulation of the refractive index opens frequency-gaps in the dispersion relation [2] which prevent the propagation of light. Because three dimensional PhCs are not compatible with standard semiconductor process technology, we use a InP/InGaAsP-slab-waveguide configuration to confine the light in the vertical direction and fabricate a two dimensional PhC in the horizontal plane. Conventional semiconductor device processing technologies can therefore be employed for the realization of waveguides with e.g. sharp bends [3] and cavities [4].

II. Mask fabrication

Our crystals consist of an InP/InGaAsP lattice-matched slab waveguide with a periodic array of etched air holes with a diameter of 210nm to 770nm.

After cleaning the surface, an intermediate mask (400nm SiO_x) was PECVD-deposited and 200nm PMMA 950K was spin-coated. The holes were then written by electron-beam lithography at 30kV with an area dose of 260µC/cm^2. Prior to writing, the proximity effects were corrected using our software tool [5]. The intermediate mask layer was dry-etched with a CHF_3/Ar plasma at a rate of 40nm/min and with a selectivity of 1:3. Typical SiO_x mask and ICP-RIE etched InP can be seen in Fig. 1 and 2 respectively.

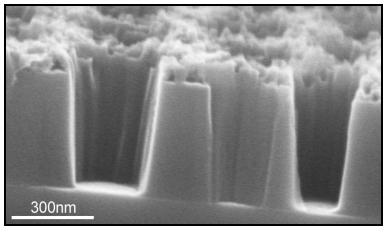

Fig. 1: SEM micrograph of a 400-nm thick SiO_x mask layer with PMMA mask residuals after 11 minutes etch time.

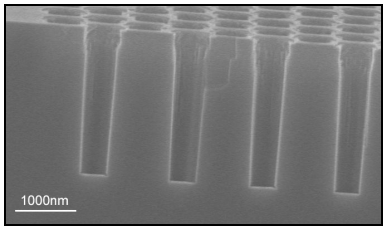

Fig. 2: SEM micrograph of etched holes in InP. Lattice constant 800nm, hole diameter 560nm. Hole depth is over 2µm.

III. Experiment and Results

After mask fabrication, the samples were etched for 2 minutes with a Plasmalab System 100 ICP-RIE from Oxford Plasma Technology under different conditions. The etching parameters are given in Table 1. Four parameters were varied over 3 equidistant levels.

Chlorine flow	5sccm	6.5sccm	8sccm
Pressure	2.5mTorr	3.5mTorr	4.5mTorr
ICP power	1000W	1300W	1600W
RF power	100W	150W	200W

Table 1: ICP process parameters. The parameters are varied over three levels according to the design of experiment matrix [6]. The methane and hydrogen fluxes are 15sccm.

The experiment was planned and analysed according to the DOE method from G. Taguchi [6]. This method reduced the experimental effort from 81 runs to a subset of 9 runs. This subset was chosen to give each input parameter the same weighting. This allows the extraction of the main contribution of

one process parameter by averaging the other parameters out.

After etching, the bulk etch depth and the selectivity against the SiO_x-mask were measured. The results are shown in Fig. 3 and agree well with our expectations. The errors were estimated to be less then 1% in the etch rate but about 30% in the etch selectivity. The large error is related to difficulties in measuring the SiO_x etch rate with profilometry.

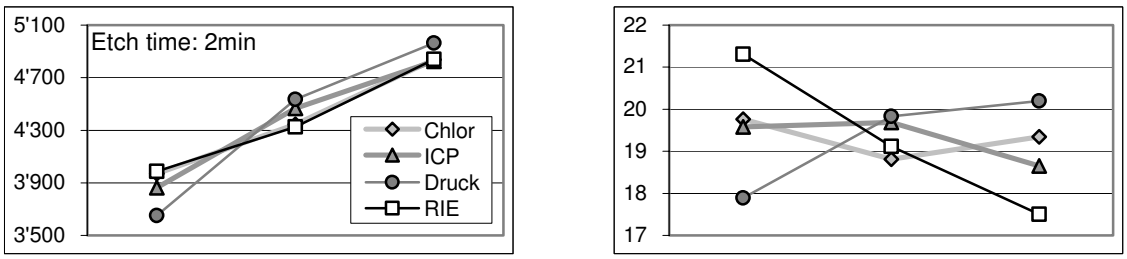

Fig. 3: Main contribution of the process parameter to InP bulk etch depth (left, total depth, [nm]) and selectivity (right). The x-axis represents the parameter variation according Table 1.

The samples were then cleaved to investigate the hole quality with a scanning electron microscope. The quality of the holes was rated for averaging with emphasis on the hole shape and the bottom of the holes.

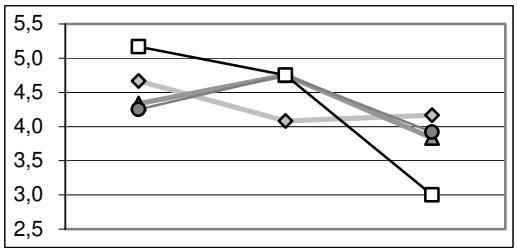

Fig. 4: Estimated rating of the holes [arbitrary units]. The x-axis represents the parameter variation according Table 1.

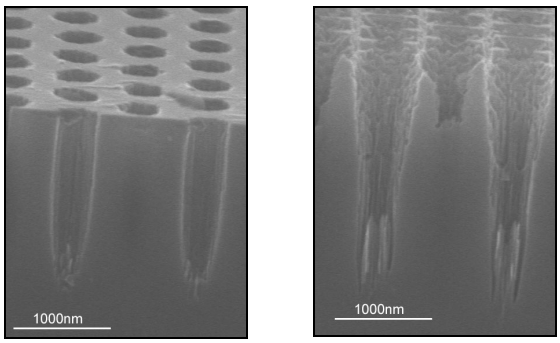

Fig. 5: Comparison of two typical holes with low (left) and high (right) RIE power (lattice constant 800nm).

As can be seen in Fig. 4, high RIE power (200W) is the main contribution to the degradation of the hole quality. The degradation seems to be related to mask erosion. Due to the qualitative rating of the holes, the influence of the other parameters cannot be determined, but there are also indications that high ICP power will erode the mask. Two typical holes can be seen in Fig. 5. Besides the root-shaped features at the bottom, the upper half of the hole etched with high RIE power shows typical features of mask erosion. Good holes over 2µm deep and with almost vertical sidewalls are achieved with low RIE and ICP power (Fig. 2).

We also observed the need for longer chamber conditioning with oxygen- and etch plasma for hole etching than for large structures. Even though the experiments were well-reproduced for bulk structures, we observed different results in hole shape when the pre-conditioning process differed.

Conclusion

We have shown that the main contribution of process parameters to the etching conditions can be extracted in few runs with the help of the Taguchi's DOE method. The achieved results for bulk etch rate agree well with the expectations. At low RIE and ICP power holes over 2µm deep with almost vertical sidewalls have been observed, but higher power seems to degrade the holes due to heavy mask erosion.

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Lasing in organic 2-D photonic band gap structures

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A circular Bragg reflector, etched in SiO_2 and coated with an active polymer, is modeled and optically characterized. The simulations and the experimental results are in a good agreement.

Introduction

To achieve a high photon confinement, optically pumped organic polymer lasers are fabricated by spin-coating a thin film of a methyl-substituted ladder-type poly(*p*-phenylene), MeLPPP, onto a nano-patterned SiO_2 circular grating surface-emitting distributed Bragg reflector [1]. Varying the period of these 2-D photonic band gap structures allows the tunability of the laser wavelength. By comparison of both the emission spectra below and above threshold in first experiments, we observed lasing spectrally located at the band edge of the Bragg dip [2]. Furthermore, in order to get a deeper insight into the underlying physics, we additionally varied the duty cycle and the diameter of the inner ring. Besides lasing at the band-edge, we observe an extra peak inside the stop band. An analytical model, based on the transfer matrix method [3, 4], has been developed in order to explore the origin of this peak. The experimental findings are compared with the theoretical results.

Model

In order to find the resonant modes in a circular Bragg reflector, we use a 2D model restrained to the in-plane aspect of the problem. This model consists of *N* concentric cylindrical layers of dielectric materials. The *E* and *H* fields must satisfy the Maxwell equations in each layer *j* and their tangential components must be continuous at all layer interfaces (1). We use complex Hankel functions $H_m^{(1,2)} = J_m \pm i\, N_m$ where J_m and N_m are the Bessel and Neumann functions and *m* is the azimuthal number. H_m' and H_m* are the derivative and the complex conjugate of the Hankel function, respectively. Calculations lead to a relation between the field coefficients in the central cavity and those outside the structure which is represented by a transfer matrix M_m^N (2).

$$\begin{cases} E_j^{\,j}(r,j) = \dfrac{i}{n_j e_0 c}\displaystyle\sum_{m=0}^{\infty}\left[a_m^{\,j} H'_m(n_j k_0 r) + b_m^{\,j} H'^{*}_m(n_j k_0 r)\right]\cdot e^{im j} \\ H_z^{\,j}(r,j) = \displaystyle\sum_{m=0}^{\infty}\left[a_m^{\,j} H_m(n_j k_0 r) + b_m^{\,j} H^{*}_m(n_j k_0 r)\right]\cdot e^{im j} \end{cases} \quad (1)$$

$$\begin{cases} \begin{pmatrix} a_m^{\,N} \\ b_m^{\,N} \end{pmatrix} = M_m^{\,N} \begin{pmatrix} a_m^{\,1} \\ b_m^{\,1} \end{pmatrix} & (2) \\ \dfrac{P_1}{\displaystyle\sum_{j=1}^{N} P_j} = \dfrac{\left|a_m^{\,1}\right|^2 + \left|b_m^{\,1}\right|^2}{\displaystyle\sum_{j=1}^{N}\left|a_m^{\,j}\right|^2 + \left|b_m^{\,j}\right|^2} & (3) \end{cases}$$

Representing the power P_j in each layer *j* using these coefficients, we can check the energy confinement by plotting the power ratio between the inner cavity (first ring) and the whole structure (3). In the graphs shown below, we plot this function (3) for a TE polarization and observe a clear peak inside the band gap. In Fig.1, eq. (3) is calculated for a circular grating with a cavity radius $R=0.5l$. In Fig.2, we vary the cavity radius and see how the wavelength of the peak changes.

λ

Fig. 1: Power ratio vs Wavelength, inner cavity radius R=1 l for m=0, 1 and 2.

Fig. 2: Power ratio vs Wavelength, inner cavity radius R=0.5 l, 1 l, 1.5 l and 5 l for m=0.

Experimental results

The circular grating structures were written into fused silica substrates by electron beam lithography and transferred by ion beam etching. The polymer film thickness is *t~120 nm*, the grating period *L=318 nm*, the number of layers *N=155* and the duty cycle $d_c=0.5$. We optically pump the structures with a frequency doubled Ti:Sapphire laser at *l = 400 nm* and collect the photo-luminescent spectra *(Fig. 3)* with a CCD camera coupled to a spectrograph. Beside the photonic band gap, we observe an evident peak as predicted by the simulations.

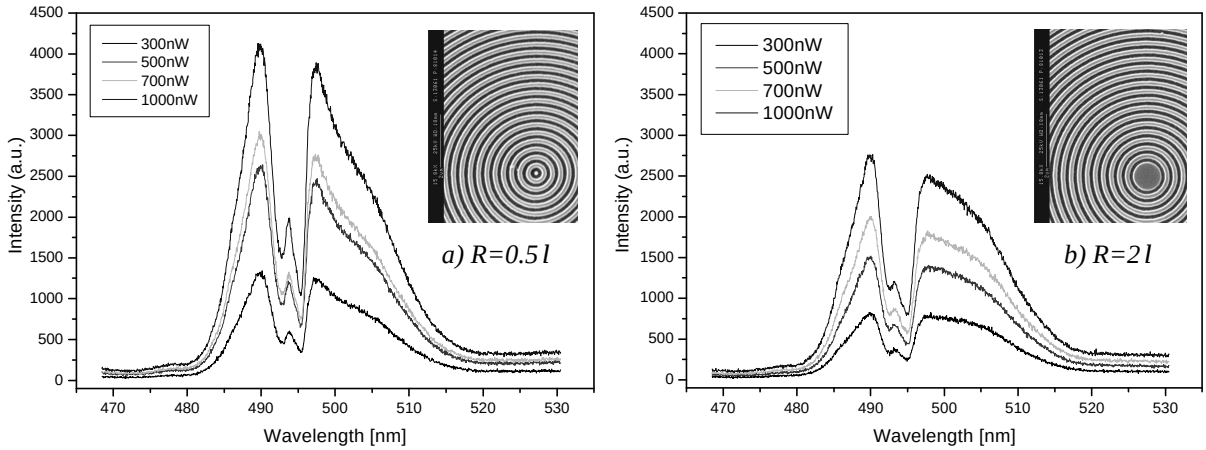

Fig. 3: SEM picture of a circular grating and its PL graph below lasing threshold. a) R= 0.5 l and b) R= 2 l.

Conclusion

We set up an analytical model based on a transfer matrix method in order to resolve the in-plane energy confinement within a circular Bragg reflector. We then compared the simulations to the experimental results which are in a very good agreement. Both results provide a good understanding of the lasing at the band edge and inside the band gap. Further investigations are planned by varying the film thickness and the chromophor density in order to maximize the energy confinement within the cavity.

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On the photoresponse of (Al,Ga)N-based UV detectors at high energy photons

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ABSTRACT

The photoresponse of AlGaN-based UV photodetectors has been studied for photons up to 600 eV by using synchrotron radiation. Spectral responses of GaN-based photodiodes were also obtained in detail in the range of 200-400 nm. It was found that registered results are affected by the presence of centres active for photons near or above bandgap. The presence of these states induces a time-dependent behaviour in the characterisation process. In addition to the detector response in the EUV range, this time-dependent performance is shown and discussed.

INTRODUCTION

(Al,Ga)N-based photodetectors have been demonstrated as an alternative to the well-established silicon sensors for photodetection in the UV range. It is expected a better operation of wide bandgap materials in aggressive environment, and a superior hardness to ionising radiations because of the high-bonding energy of the atoms in these semiconductors. Traditional solid state detectors show other shortcomings which are not present in wide bandgap materials, like the need of filters, cooling and a poor contrast between UV and VIS/IR radiation. However, the material quality of these novel wide bandgap materials is not good enough yet. The lack of dislocation-free GaN bulk substrates and the high density of native defects are the main issue. Among the challenges of EUV detection one may point out high material absorption at this range that forces to take a very special care of surface properties. Furthermore carrier trapping can affect the electronic transport, and therefore the level of the photocurrent signal and its time response. In this paper we summarize the results of the photoresponse characterisation under high energy photon irradiation for a wide set of (Al,Ga)N samples.

EXPERIMENTAL AND RESULTS

Schottky barrier and metal-semiconductor-metal (MSMs) photodetectors were fabricated, with areas ranging 100 μm to 500 μm of diameter (for circle shape devices) and 250x250 μm^2 to 500x500 μm^2 respectively. Detectors were processed on samples grown by MOCVD and by MBE using sapphire and silicon (111) substrates [1][2]. MSMs consist of two interdigitated electrodes on a planar structure with finger widths and gap spacing of 2, 4 and 7 μm. Contacts were made using Ti (300 Å)/Al (700 Å) and Ni (300 Å)/Au (1000 Å). Schottky barrier photodiodes consist of a planar structure where the active area is circular, and the contacts used in the fabrication were Ni (300 Å)/Au (1000 Å) for the rectifying contact and Ti (200 Å)/Al (1000 Å)/Ti (450 Å)/Au (550 Å) for the ohmic contact. Photoresponse measurements in the range of 200 nm and beyond were performed by using a 150 W Xe arc lamp as a source and a monochromator system. In order to obtain the responsivity, the relative spectral response of the system was measured by a calibrated Molectron PR200 pyroelectric detector. High energy measurements in the EUV ranges were carried out by using the synchrotron facilities of LURE in Orsay (Paris).

Results in Figure 1 indicate that $Al_xGa_{1-x}N$ metal-semiconductor-metal photodetectors show good sensitivity at high energy photons. The samples characterised between 10 and 150 nm were grown by MOCVD with Al content of 14% and 27%. Since the photoresponse of the MSMs was bias-dependent, no conclusions could be obtained about the relationship between aluminium fraction and photoresponse. Theoretical predictions suggest that the ionisation energy, which is the average amount of radiation consumed per electron-hole pair, should increase with Al content so quantum efficiency should be lower [3]. In the inset included in Figure 1, the photoresponse of the MBE $Al_{0.02}Ga_{0.98}N$ photodetector allows the identification of the C-edge transition [2]. Schottky barrier photodiodes processed in GaN samples were characterised in the range of 200-400 nm for photovoltaic operation.

In Figure 2 a typical relative response is shown. In contrast to MSM photodiodes, the use of a semitransparent contact layer (transmittance below 40%) may deteriorate the photoresponse of those wavelengths [4].

In the responsivity measurements it was also observed the presence of slow time-dependent response (Figure 2). This strongly suggests that a high concentration of traps seems to be affecting the level of the photocurrent signal. According to transient photocurrent responses measured for undoped GaN samples and capacitance data as a function of wavelength, the defect states responsible for the time-dependent behaviour should be one which is close to the valence band, E_{t1}, (≈150-200 meV) and another which must be empty inside the depletion region, E_{t2} (in order to capture electron carriers). The dependence of the transient effect with optical power and temperature was studied. Optical power was proved to be the main mechanism to control the shape and magnitude of the transient because the optical emission and capture (through the increase of carrier density) rate for electrons depends on the photon flux. Temperature-dependent measurements revealed that refilling of the valence band traps is a thermal controlled process. However, measurements made under background visible light showed that refilling can be also optically produced (Figure 2).

CONCLUSIONS

In summary, the photoresponse of (Al,Ga)-N based photodetectors was presented, where MSMs showed better performance than Schottky barriers for high energy photons. Additionally, the presence of time-dependent phenomena, which influences the final registered photoresponse, was observed in n-type samples from different sources.

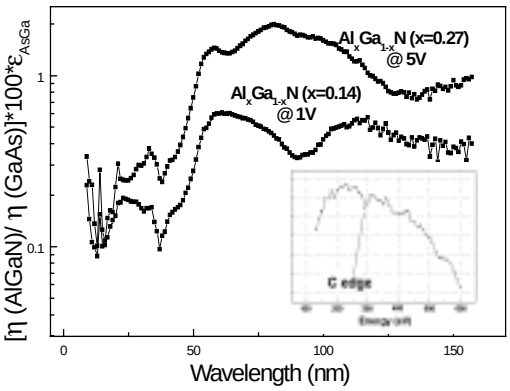

Fig.1. Optical response of the AlGaN metal-semiconductor-metal photodetectors to the synchrotron radiation.

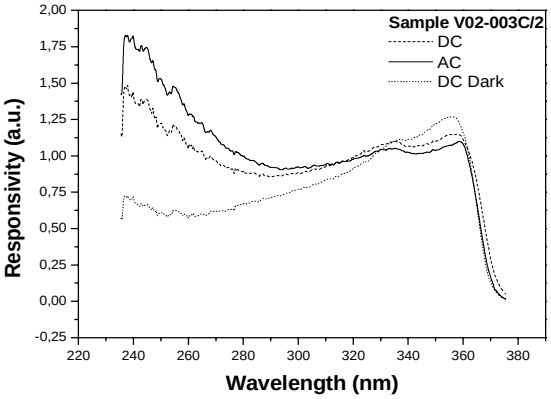

Fig.2. Dependence of the photoresponse on the measurement conditions for GaN Schottky barrier photodiodes.

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Photoluminescence of the AlGaN/GaN heterostructure and two-dimensional electron gas

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Photoluminescence (PL) of modulation-doped $Al_{0.12}Ga_{0.88}N$/GaN heterostructures was investigated. The PL peak related to recombination between the two-dimensional electron gases (2DEG) and photoexcited holes is located at 3.529, 3. 552 and 3.564 eV depending on the thickness (d) of the unintentionally AlGaN (i-AlGaN)-space layer at 10K. The 2DEG density at the heterointerface increases with increasing temperature, the red-shift of the 2DEG peak is smaller than of the D^0X peak in the GaN layer as temperature increases.

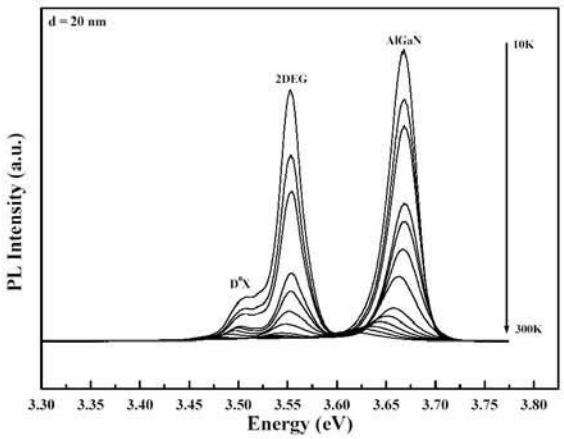
Introduction – Design – Experimental Verification

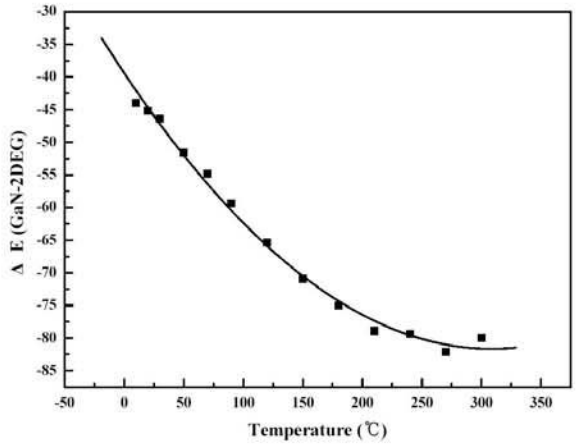
Presently, AlGaN/GaN heterostructres have attracted much attention due to the potential for application in high-power, high-temperature microelectronic devices.[1-2] The large band offset and strong piezoelectric effect in this material system have been shown to induce a high sheet density two-dimensional electron gas (2DEG) with an enhanced electron mobility. Several groups have presented the 2DEG photoluminescence (PL) spectra of AlGaN/GaN heterostructures.[3-4] There have been a number of studied aiming at the understanding of the transport properties of AlGaN/GaN heterostructures; very little work has been reported about the optical properties of AlGaN/GaN heterostructures. In this letter, we present the growth and optical studies of AlGaN/GaN heterostructures and the thickness of the spacing layer of AlGaN barrier were investigated. Also, this letter elucidates the 2DEG subband photoluminescence spectra and their temperature dependence in detail for various high-electron-mobility transistor (HEMT) structures, which have not been clearly resolved in the literature.

Modulation-doped AlGaN/GaN heterostructures were grown by atmospheric pressure metal-organic chemical vapor deposition (MOCVD). The composition of aluminum in the AlGaN layer was determined as 12% by using X-ray diffraction (XRD) analysis. Strain and relaxation of the AlGaN layer on GaN were analyzed by means of PL. The PL spectra at various temperatures were obtained by 325 nm He-Cd laser excitation.

The PL spectra of a modulation-doped AlGaN/GaN is shown in Figure 1(a) at different temperatures. The spectra is dominated by 2DEG emission at 3.552 eV in low temperature. Figure

1(b) shows the energy separation of 2DEG peak position from the D^0X emission of GaN with different temperatures from 10 to 300K. The 2DEG density at the heterointerface increases with increasing temperature. This makes the triangular potential well in the conduction band edge at the heterointerface become a little shallower due to increased screening and a consequent reduction in the space-charge potential, which originates from both the conduction band discontinuity and the piezoelectric charges at the AlGaN/GaN interface.[5] Thus, the red-shift of the 2DEG peak is smaller than that of the D^0X peak as temperature increases.





Conclusion

We have investigated the growth and optical properties of AlGaN/GaN heterosturctures. The PL peaks related to recombination of between 2DEG and photoexcited holes observed at the photon energy range between the GaN and AlGaN band gap and their origin and nature are discussed.

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Technologies for Power MMICs

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UMS has been involved in the development technologies for power applications since its creation. The domains of application encompass all frequency bands between 1 to above 40GHz, and a very wide range of products including military as well as commercial applications. In order to achieve such a wide spectrum and still be able to offer state-of-the art performances a large variety of technology versions were developed using GaAs-based PHEMT as well as HBT devices. However, ever increasing requirements already imposes further improvements, and UMS is already strongly involved in the development of an AlGaN-GaN PHEMT technology. This paper will give an overview of the results already achieved in the field of power technologies, and show some results from the on-going activities regarding GaN PHEMT devices.

UMS has been involved in the development of an HBT technology for X-Band applications since its creation, building in the already extensive experience inherited from its mother companies [1,2,3]. Logically the first product based on this process was an X-Band power amplifier. Fig. 1 shows typical performances obtained with this circuits. One major obstacle to the commercial application of this process has long been its reliability. Through a very thorough optimization of the process however it was possible to improve the lifetime of the devices to reach the million-hour mark, and therefore meet even the toughest requirements [7,8]. This process, called HB20P, has even successfully gone through a space evaluation. Further evolution of the process also included the optimization of thermal bump in order to allow the application of the devices in flip-chip configuration [4,5]. Fig. 3 shows an SEM view of such a device. Fig. 2 shows Gummel plots. At the same time other versions of the process have been developed to address other applications. In particular, a very high voltage version is being developed for S-band and L-band applications like radar, base-station and space applications, with typical bias conditions up to more than 20V [10, 11, 13]. Figure 4 and 5 show an SEM view an output characteristics of such a power device. Such devices can deliver up to 9W at 2 GHz (Figure 6), and when combined they allow the fabrication of single chips delivering up to 30W. These are chips are then used as building block for the realization of power modules in the 100W range.

In parallel, PHEMT technologies were developed for power applications from Ku up to Ka-Band [12]. For example Figure 7 to 11 shows results obtained on circuits designed for VSAT applications in these two frequency bands. By optimizing design concepts and by using advanced process approaches it was possible to significantly reduce chip size for a given output power and thus to achieve very high Pout-per-unit-chip-area ratios. These results are twice as high as previously reported values at Ka-Band.

Finally, in order to prepare the next generation products necessary for future for military as well as for commercial applications UMS is actively involved in the development of GaN-based devices. In particular, cooperations have been started with all major research institutions involved in this field around Europe. Already, these efforts have allowed state of the art results [15]. Si Substrates offer a very attractive alternative SiC for power applications. Cost and manufacturability would especially benefit from the successful development of an AlGaN/GaN HEMT technology on Si. Figure 11 shows the power performance of 2x125µm device fabricated on MBE-grown layers on Si. This result represents the highest power density published so far on such devices.

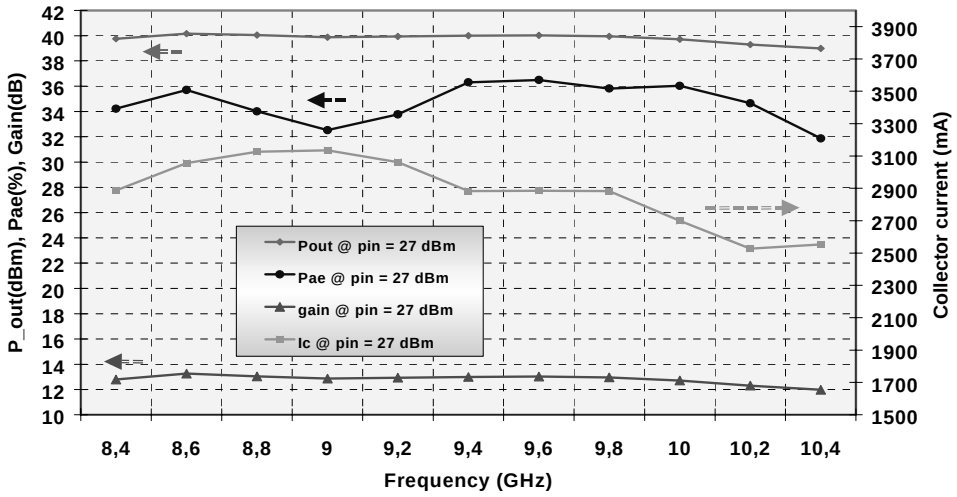

Fig. 1: Power performances of a 10W X-band HPA MMIC (CHA7010)..

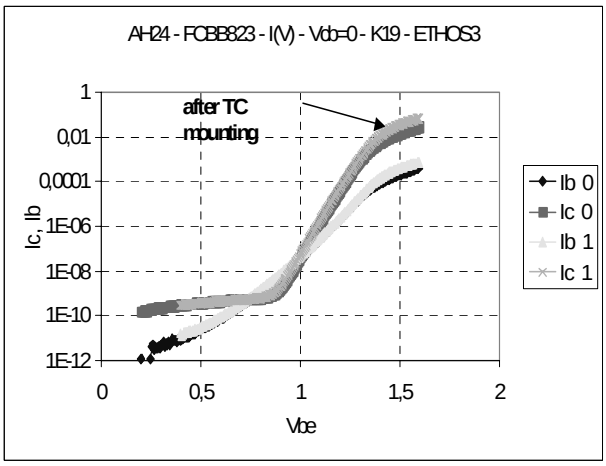

Fig. 2: Typical Gummel plot obtained on InGaP based HBT (8 finger HBT with 2x30 µm^2 emitter area before and after flip-chip assembly).

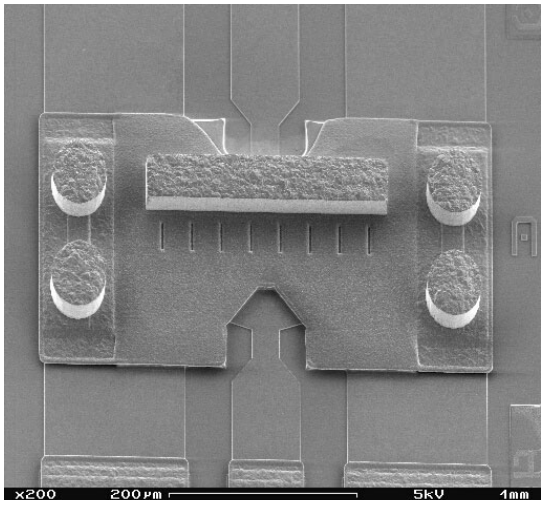

Fig. 3: SEM picture of Heterostructure Bipolar Transistor in CPW topology with thermal bumps on top of the HBT active area

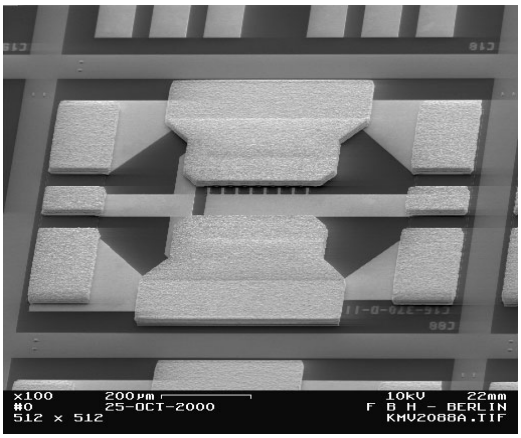

Fig. 4:: SEM image of HBT power cell.

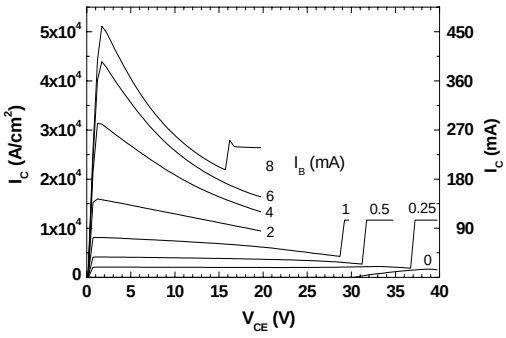

Fig. 5 I-V characteristics of 10 emitter finger HBT (10x3x30 µm^2) with base current I_B as parameter.

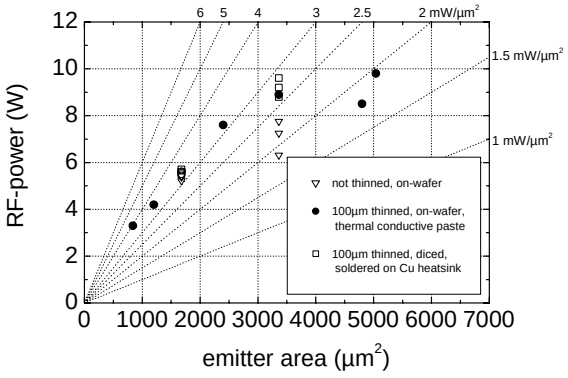

Fig. 6: RF output power of HBT power cells in dependence on total emitter area and for different heatsinking conditions measured at collector bias of 26 V and at 2 GHz and for different heatsinking conditions.

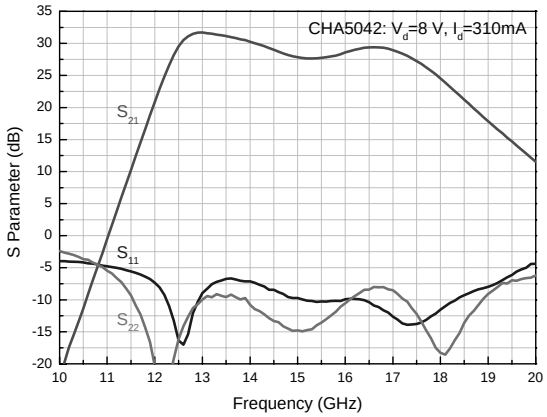

Fig. 7: 29-dBm Ka-band VSAT PA – PPH25x (1.9mm² - CHA5042)
Vds = 8Volt / Ids = 310mA

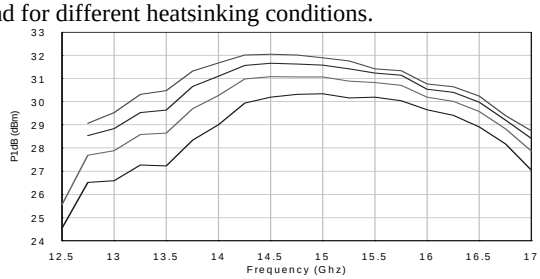

Fig.8: 31-dBm Ku-band VSAT HPA – PPH25x (3.3mm² - CHA6042) (Vds = 6, 7, 8, and 9V respectively)

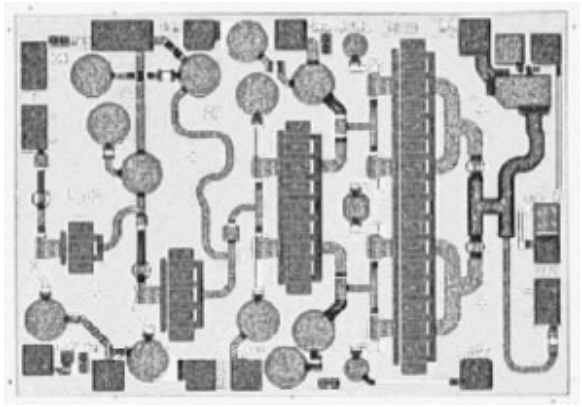

Fig. 9: Pa-PO9981 VSAT Ka-Band PA – PPH25 (2.47 mm²)

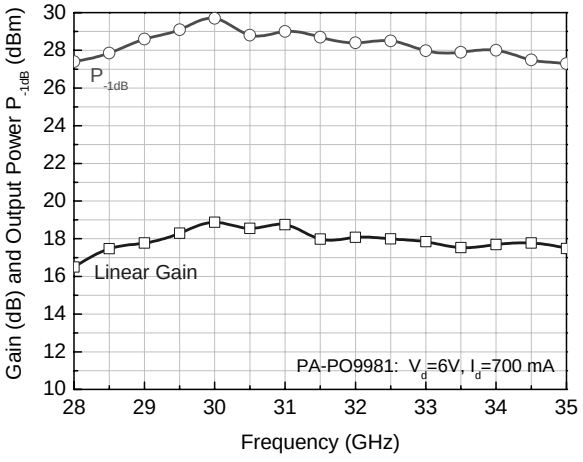

Fig. 10: VSAT Ka-Band PA – PPH25 (2.47 mm²)
Vds = 6Volt / Ids = 700mA

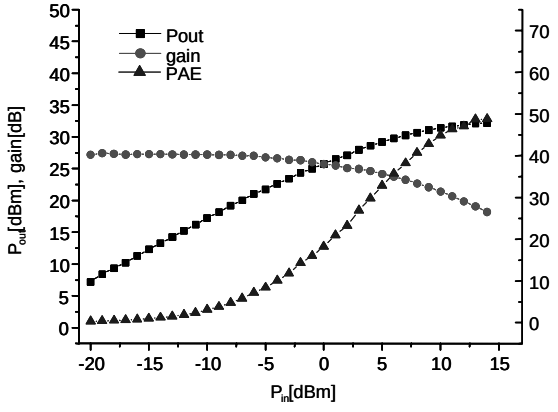

Fig. 11: Class AB power measurement of a 2x125µm AlGaN/GaN HEMT on silicon substrate. VDS=30V, Poutmax=32.18dBm, PAE at Poutmax 49%.

Acknowledgments

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Comparison between lattice matched and strained channel InP HEMTs at room and cryogenic temperature

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The performance of lattice-matched and strained-channel InP HEMTs are presented. The peak transconductance of devices with a strained channel shifts in the order of 44% at room and cryogenic temperatures. The cutoff frequency shows a more pronounced enhancement at cryogenic than at room temperature. Additionally we show that the noise is reduced.

Introduction

In certain applications like radio-astronomy and deep-space communication, there is a need for receivers with high sensitivity and ultra low noise. Most receivers in these applications make use of cryogenic amplifiers with InP HEMTs in the front end [1], operating within C, X and K bands.
The goal of this work is to achieve an improvement of the gain and noise performance of the device, which directly influences the sensitivity of the receivers. In this paper, we present a comparison of lattice-matched and strained-channel InP HEMTs. Dc and rf measurements have been carried out at room and cryogenic temperatures.

Device structure and fabrication

The HEMT structures studied in this work are as follows: n-doped $In_{0.53}Ga_{0.47}As$ cap, $In_{0.52}Al_{0.48}As$ Schottky barrier, Si-δ doping plane, $In_{0.52}Al_{0.48}As$ spacer, $In_xGa_{1-x}As$ channel, $In_{0.53}Ga_{0.47}As$ pre-channel, and $In_{0.52}Al_{0.48}As$ buffer. The first structure consists of a lattice matched InGaAs channel and the second structure consists of a strained $In_{0.70}Ga_{0.30}As$ channel.
The devices have a gate length of 0.2μm and a gate width of 2×75μm. The T-shaped gate was defined by an electron beam lithography process with a triple PMMA-based resist-layer stack. Gate recess through the $In_{0.53}Ga_{0.47}As$ cap layer was done using a highly selective wet-chemical etching process. A cross-section of the device is shown in Fig. 1.
Due to a higher Indium content in the InGaAs channel of the strained layer devices, the mobility increases at room and cryogenic temperatures (see Table 1). Additionally, a better carrier confinement can be reached. This translates into higher transconductance and higher cutoff frequency.

Measurements

The devices were characterized using an on-wafer cryogenic probe station. The probe station consists of a wafer probing system, vacuum pumps, open-cycle cooling apparatus, and a microscope. The vacuum chamber contains a copper chuck on a cold finger, temperature sensors, and microwave probes attached to manipulators through metal bellows.
The devices were first measured at room temperature and then cooled down to cryogenic temperature. Figures 2 and 3 shows the extrinsic transconductance of the lattice-matched and the strained-channel HEMTs, respectively, measured at 300K, 77K, and 10K. The peak transconductance of the devices at different temperatures is summarized in Table 2. Thanks to the strained channel the transconductance is increased by 42% to 45% at room and cryogenic temperatures. The improvements are similar even though there is a more pronounced shift in the mobility at cryogenic temperature due to the strained channel. Additionally, a shift of the threshold voltage V_{th} can be observed for both device structures when cooling the devices (see Table 3). This behavior is believed to be generated by the lower donor ionization at lower temperature.
The S-parameters were measured at room and cryogenic temperatures from 0 to 40 GHz at a bias point of V_{ds}=0.5V and I_{ds}=5mA. At this bias point, typical for low-noise applications, the improvement of f_T was measured to be 40% to 60% upon cooling both devices from room to cryogenic temperature. Comparing the influence of the In content in the channel, the increase of f_T is more pronounced at cryogenic temperatures as can be seen in Table 4. For devices biased near the peak transconductance, a similar analysis in [2] showed a larger change of the cutoff frequency in function of strain.

The noise performance is a main criterion governing the choice of a device used in very sensitive receivers. The noise measurements were performed under the bias condition of V_{ds}=0.5V and I_{ds}=10mA at room temperature. The measured minimum noise figure F_{min} is shown in Fig. 4. The improved noise performance of the strained-channel HEMT is believed to be due to a combination of reduced intersubband and alloy scattering mechanisms.

Conclusion

The dc, rf and noise characteristic of lattice-matched and strained-channel HEMTs have been investigated. The performance improvement of strained-channel HEMTs is particularly pronounced at cryogenic temperatures whereas a significant enhancement could be already observed at room temperature. In order to further investigate the effect of the strained channel on the overall device performance, LNAs will be developed and characterized at room and cryogenic temperatures.

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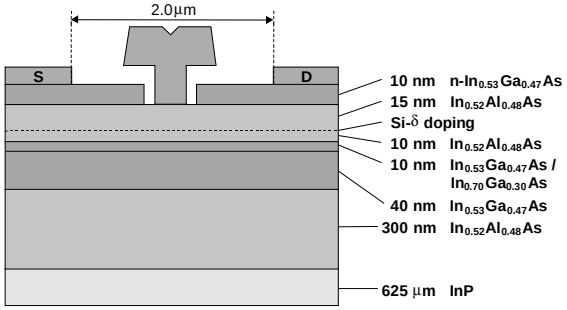

Fig. 1: Cross-view of 0.2µm InP based HEMT device

	300K	77K
$In_{0.53}Ga_{0.47}As$	10'300	34'500
$In_{0.70}Ga_{0.30}As$	12'600	68'600

Table 1: Measured Hall mobility [cm^2/Vs]

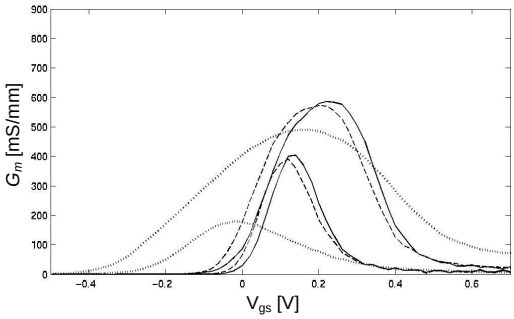

Fig. 2: Lattice-matched InP HEMT at 300K (dotted), 77K (dashed) and 10K (solid)

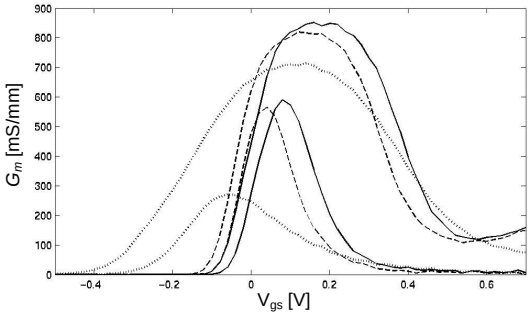

Fig. 3: Strained-channel InP HEMT at 300K (dotted), 77K (dashed) and 10K (solid)

	300K	77K	10K
$In_{0.53}Ga_{0.47}As$	495	575	585
$In_{0.70}Ga_{0.30}As$	705	820	850
$G_{m,max}$ improvement	42 %	43 %	45 %

Table 2: Measured $G_{m,max}$ [mS/mm]

	300K	77K	10K
$In_{0.53}Ga_{0.47}As$	-0.35	-0.06	-0.02
$In_{0.70}Ga_{0.30}As$	-0.36	-0.10	-0.08

Table 3: Measured V_{th} [V]

	300K	77K	10K
$In_{0.53}Ga_{0.47}As$	82	114	121
$In_{0.70}Ga_{0.30}As$	89	136	142
f_T improvement	9 %	19 %	17 %

Table 4: f_T at bias point V_{ds}=0.5V, I_{ds}=5mA [GHz]

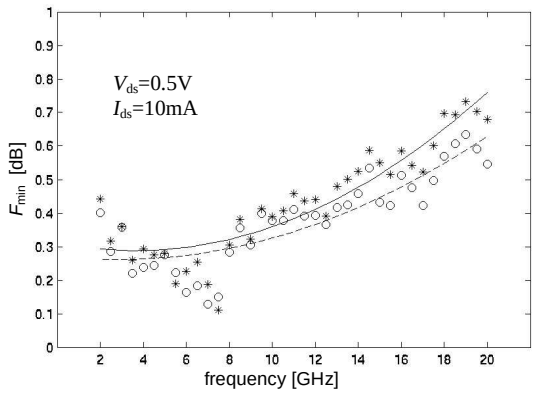

Fig. 4: Measured F_{min} at 300K for lattice-matched (solid) and strained-channel (dashed) InP HEMTs

Frequency transconductance and Gate-Lag dispersion in InAlAs/InGaAs/InP HEMTs

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The aim of this paper is to sistematically study dispersion effects in various InP HEMT technologies, with and without InP etch-stop, and with different recess widths, by means of a wide set of techniques, including frequency transconductance dispersion, gate-lag and drain-lag transient measurements, current Deep Level Transient Spectroscopy (DLTS). Results demonstrate that two-step recess devices adopting InP etch-stop layer and optimized Schottky contact on InAlAs are free from dispersive and kink effects even with very wide gate recess widths (400 nm) and extremely short gate lengths (30 nm).

For high-speed optical fiber communication systems and extremely high-frequency wireless systems, InP-based High Electron Mobility Transistors (HEMTs) currently represent the most promising electronic devices [1]. Current gain cut-off frequency (f_T) reached 340 GHz in 1992 [2] and 400 GHz in 2001 [3]. In the course of the 1990's, several improvements to device technology have been developed, resulting in optimized structures for deep sub-0.1 μm-gate InP HEMTs, including improved recessed-gate structures [4], engineering of the gate contact [1],[5], adoption of an InP etch-stop layer on the device surface [1],[5], of a two-step recess gate [1], substitution of the InAlAs donor layer with an InP donor layer in order to eliminate degradation due to fluorine contamination [6]. In particular, adoption of the InP etch stop layer for gate recessing has significantly improved the uniformity and reproducibility of the threshold voltage and transconductance of HEMTs [7]. The surface passivation effect of the InP layer eliminates kink effects, and alleviates frequency dispersion and hot-electron aging effects [8]-[10]. Placing the gate Schottky contact directly on top of the InP etch-stop layer results in high gate leakage current due to the low Schottky barrier height; a two-step structure has the gate metal deposited on the InAlAs barrier, and the InP etch-stop layer in contact with the edge of the gate metal, so that the recess region has a large conductivity due to its large carrier concentration.

The investigated devices are InAlAs/InGaAs/InP HEMTs fabricated by Nippon Telegraph and Telephone (NTT), see Fig. 1: **(A)** devices WITHOUT the InP etch stop layer with WIDE (0.1μm) gate recess regions; **(B)** devices where a previously InP layer grown has been removed in the access region by a subsequent process step with WIDE **(B1)** and NARROW **(B2)** (0.02 μm) recess**; (C) TWO-STEP** devices WITH the InP stopper with WIDE gate recess regions: in these devices the InP layer is removed under the gate contact with a two step gate recess process.

Results generally show a good correlation between the various measurements, i.e. frequency dispersion of transconductance is correlated with gate-lag effects, current collapse of I-V characteristics at high frequency, kink phenomena and presence of DLTS peaks. Results can be summarized as follows: (a) all devices having narrow gate recess present little or no dispersion effects, at the expenses of increased hot carrier effects and reduced breakdown voltage, see Figures 2-5; (b) dispersion effects increase at increasing gate recess width and at decreasing gate length; (c) at a recess width of 100 nm all devices having InAlAs recess surface present dispersion effects while two-step devices having InP-etch stopper show almost no dispersion effects down to a gate length of 30 nm with a recess width of 400 nm (see Figures 2-5).

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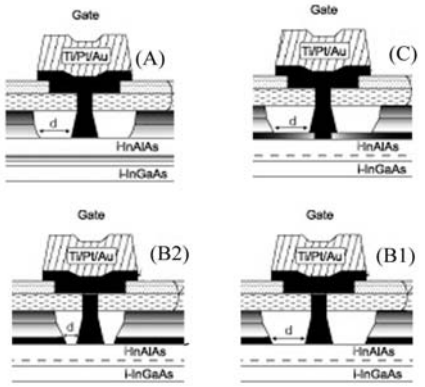

Fig.1 : Schematic cross section of the InP based HEMT's gate recess for (A), (B) and (C) devices

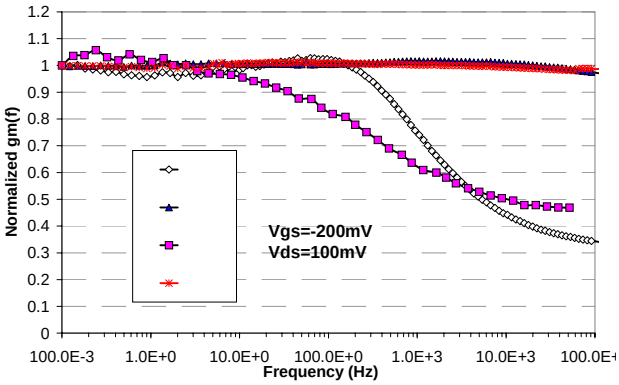

Fig2: gm(f) dispersion for (A), (B), (C) devices. Vds=100mV (linear region) and Vgs=-200mV

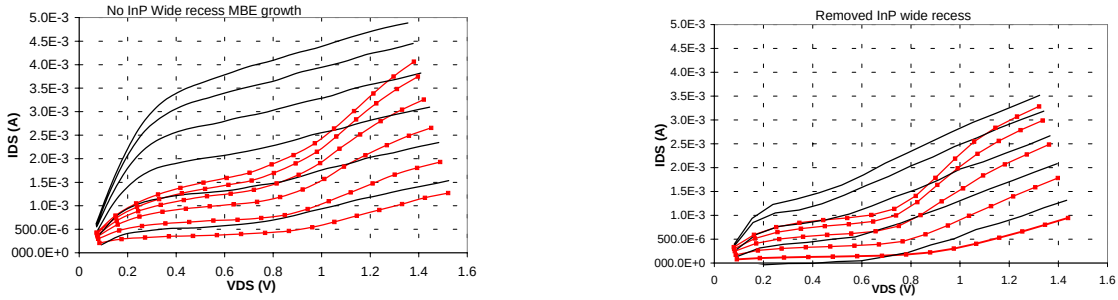

Fig 3: Gate-lag output measurements; comparison between the DC output (straight line) and Gate pulse turn on measurements(dotted line) for **(A)** (on the left) and **(B1)** (on the right) devices. Pulse width is 250ns. Vgs goes : (A) from -600mV to -100mV step 100mV; (B1) from -500mV to 100mV step 100mV

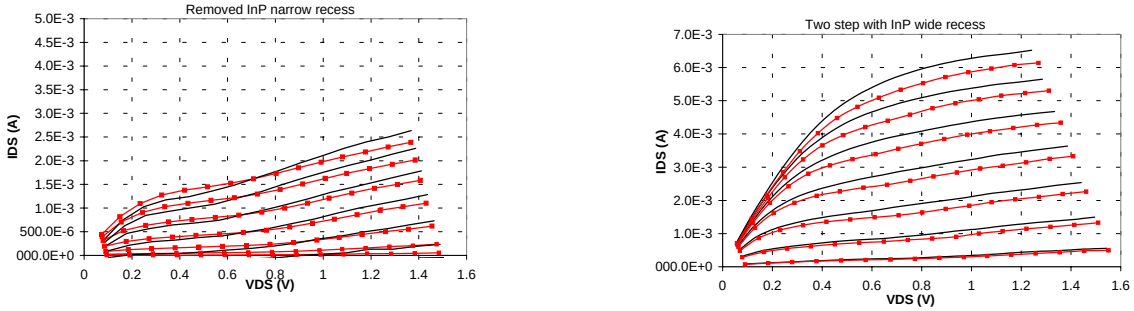

Fig 4: Gate-lag output measurements; comparison between the DC output (straight line) and Gate pulse turn on measurements(dotted line) for **(B2)** (on the left) and **(C)** (on the right) devices. Pulse width is 250ns. Vgs goes : (B2) from -500mV to 100mV step 100mV

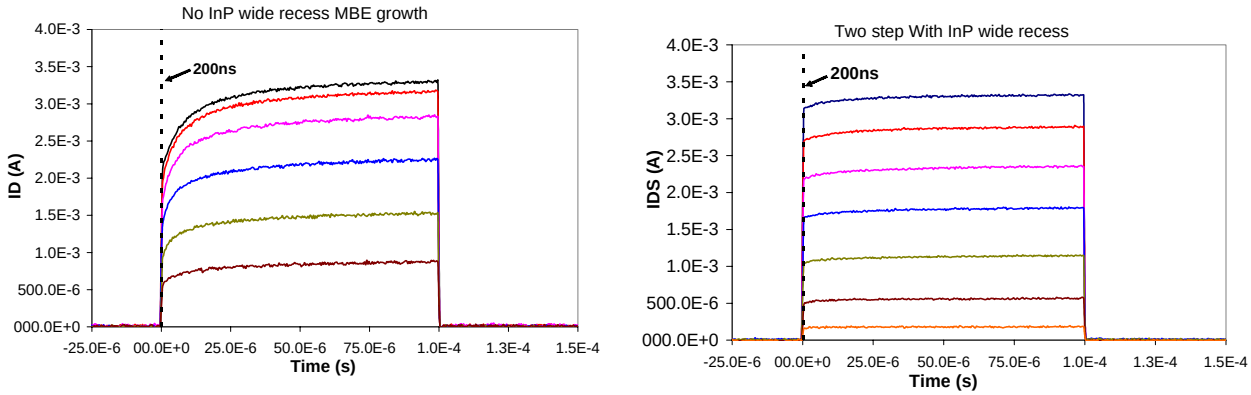

Fig 5: Gate lag turn on current pulses (100µs wide) for **(A)** (on the left) and **(C))** (on the right) devices at different bias conditions

Fabrication of InAlAs/InGaAs heterojunction bipolar transistors using self-aligned process

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This paper describes the DC electrical characteristics of InAlAs/InGaAs heterojunction bipolar transistors (HBTs) having abrupt and graded base-emitter (BE) junctions. The HBTs have been fabricated using self-aligned triple-mesa etch process. The graded junction HBT shows higher current gain and lower offset voltage as compared to abrupt junction HBT.

Introduction

Heterojunction bipolar transistors based upon III-V semiconductors are potentially very useful in high-speed and microwave integrated circuits. In an HBT, the emitter is composed of a wide-bandgap semiconductor while the base is made up of low-bandgap material. For *npn* transistors this leads to band offsets at the heterointerface that favours the injection of electrons into the base while retarding the hole injection into the emitter. This allows the base to be more heavily doped than the emitter resulting in low base resistance and emitter-base capacitance, both of which are required for high frequency operation.

Experimental

For the fabrication of the HBTs, the **$In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$** material system has been used. The HBT layers are grown lattice-matched by MBE technique on semi-insulating InP (100) substrates. The epitaxial layer structure consists of a 1000 nm InGaAs:Si subcollector layer doped at 5×10^{19} cm^{-3}, a 700 nm InGaAs: Si collector layer doped at 1×10^{16} cm^{-3}, a 80 nm InGaAs:Be base layer doped at 5×10^{19} cm^{-3}, a 100 nm InAlAs:Si emitter layer doped at 5×10^{17} cm^{-3}, a 45 nm InAlAs:Si emitter cap layer doped at 5×10^{19} cm^{-3}, and a 75 nm InGaAs:Si emitter cap layer doped at 5×10^{19} cm^{-3}. Since for an abrupt junction of $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$ there exists a spike in the conduction band, which hinders the electron flow, epitaxial material with graded junction from emitter to base has also been fabricated. For this purpose a superlattice structure of InAlAs/InGaAs having total thickness of 48 nm and doped n-type up to 5×10^{17} cm^{-3} is inserted between the emitter and base layers. The superlattice structure is comprised of three parts, each part having 8-period superlattice with thickness of 2.0 nm per period. The thickness of InAlAs and InGaAs layers in each period of the three parts are (starting from base side): first part, 0.5 nm and 1.5 nm, second part, 1.0 nm and 1.0 nm, and third part, 1.5 nm and 0.5 nm, respectively.

Test structures for the HBTs have been fabricated using a self-aligned triple mesa-etch process. This technique minimizes the distance between base and emitter contacts and moreover, isolation of the individual devices can also be achieved [1]. The etching of the various epitaxial layers in order to reach down to base, subcollector and SI-InP substrate is performed using selective and nonselective wet chemical solutions. E-beam evaporated Ti/Au (20 nm/200 nm) is used to make ohmic contacts to the emitter cap, base and subcollector. The individual metal contacts serve as etch masks for the wet chemical etching of the corresponding mesa structures.

Results and discussion

DC current-voltage measurements have been performed on the devices with the help of an HP 4142B modular DC source/monitor and Agilent's IC-CAP as data acquisition and analysis software. Gummel plot and output characteristics for an abrupt junction HBT are shown in Figs. 1 and 2 (solid lines), respectively. The current gain β of the transistor in the high current region is about 15. However, there exists an intersection of the emitter and base current that limits the application for base-emitter voltages above 1 V. The ideality factor for the base current n_B is 2.05 while the ideality factor for the collector current n_C is 1.15. The offset voltage and knee voltage, as extracted from the output characteristics, are 0.65 V and 0.90 V, respectively. The high value of n_B is indicative of the

dominance of recombination current at the base and is possibly due to the outdiffusion of Be from base to emitter [2] and/or due to the defects at the emitter-base interface. In the case of InAlAs/InGaAs transistors it has been observed using secondary ion mass spectroscopy (SIMS) that in abrupt BE junctions, there is a remarkable outdiffusion of Be from the base to the emitter [3]. The extent of diffusion depends upon the growth temperature and the concentration of the Be dopants in the base.

Gummel plot and output characteristics for the graded junction transistor are shown in Figs. 1 and 2 (dashed lines), respectively. The current gain for this structure is about 30 for high currents, i.e., twice as compared to the abrupt junction transistor and there is no intersection between base and emitter current in the Gummel plot. The values of n_B and n_C are 1.25 and 1.05, respectively. Hafizi *et al* [3] showed that the finite strain resulting from a superlattice at the BE junction prevents interstitial Be diffusion. Furthermore, in our case the growth temperature during the epitaxial growth of superlattice was about 20 K less in comparison to the growth temperature during epitaxial growth of emitter in case of abrupt junction transistor. These effects are responsible for the improvement of DC characteristics of graded junction transistor. Similarly, the offset voltage and knee voltage are also reduced and values of 0.15 V and 0.40 V, respectively, are achieved. This reduction is due to the smoothening of conduction band at emitter-base junction.

Conclusions and outlook

The InAlAs/InGaAs HBTs have been fabricated using abrupt and graded emitter-base junction epitaxial layer structures. The current gain of the transistor with abrupt BE junction is 15 while that of the one with graded junction is 30. Similarly, the offset voltage of the abrupt BE junction transistor is 0.65 V while that of graded BE junction transistor is 0.15 V. Now we will focus our efforts on the fabrication of small dimension HBTs (emitter: 2×10 μm^2 to 5×20 μm^2) for CPW circuit oscillators.

Acknowledgement

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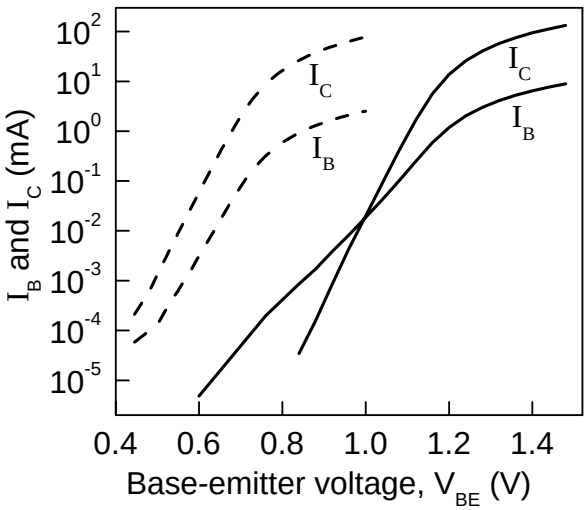

Fig. 1: *Gummel plots for abrupt (solid line) and graded (dashed line) junction AlInAs/GaInAs HBTs having emitter dimensions of 50×50 μm^2.*

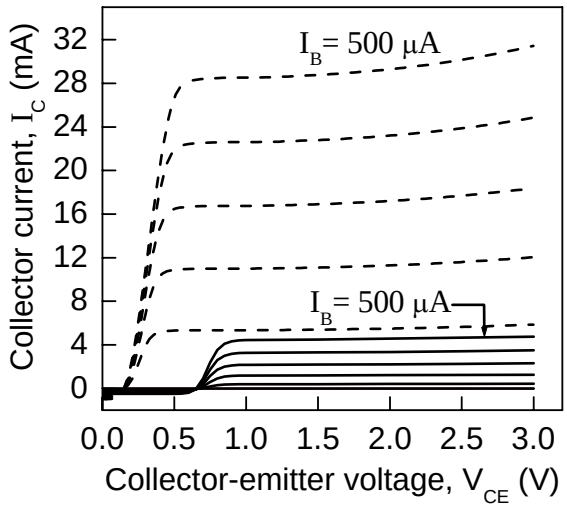

Fig. 2: *Common-emitter I_C-V_{CE} characteristics for abrupt (solid line) and graded (dashed line) junction AlInAs/GaInAs HBTs having emitter dimensions of 50×50 μm^2. The base current I_B is varied from 0 to 500 μA in steps of 100 μA for both the HBTs.*

Impact of the Number of Inverters on the Measurement of the Gate Delay of an InP HBT-Based Ring Oscillator

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Abstract

Gate delay is an important figure of merit for monitoring the fabrication process and switching speed of InP HBTs. It is shown analytically that the switching time of an inverter within an InP HBT-based ECL (emitter-coupled logic) ring oscillator stays almost constant even for a low number of n inverters while it decreases for a CML (current-mode logic) ring oscillator. This behavior can be explained by the lower voltage swing due to a lack of sufficient time to fully charge all capacitors during the switching event. Therefore, the CML-inverter gate delay would be underestimated by measuring the ring oscillator frequency $f_{\rm osc}$ with a low number of inverters and subsequently calculating the propagation delay as $t_g = 1/(2nf_{\rm osc})$. We show inverter switching times of CML and ECL ring oscillators with different numbers of inverters, based on an analytical approximation and SPICE simulations.

I. Current-Mode Logic (CML) Inverter

A ring oscillator consists of a ring of n inverters. The schematic circuit of a CML inverter and its large-signal model are shown in Figures 1 and 3. An analytical model has been developed to predict the gate-delay behavior versus number of inverters and has been compared to a SPICE circuit model [2]. The most important SPICE transistor parameters of the InP-InGaAs double HBT (DHBT) are listed in Table 1 [1]. All capacitors in all large-signal models in this paper have their values calculated with SPICE equations at dc bias [4]. $C_\mu = C_{jc}(0)$ is the base-collector capacitance. The base-emitter capacitance C_π is the sum of the base-emitter depletion capacitance in forward bias $C_{je} = C_{je}(0)(1+m_e)$ and the diffusion capacitance $C_D = \tau_f g_m$, where $g_m = \Delta U_{BE}/\Delta I_C = V_h/I_{EE} = 1/R_L$, and $V_h = R_L I_{EE}$ is the voltage swing [3]. $R_\pi = \beta/g_m$ and $I_{gm} = I_{EE}/2 \cdot \tanh(U_{\pi 1}/2U_T) = g_{m,nl}U_{\pi 1}$ is nonlinear due to the conductance term $g_{m,nl}$ ($U_T = kT/e$) [3]. As $U_{\pi 1}(t)$ is periodic with the oscillation frequency $f_{\rm osc}$, we may split $U_{\pi 1}(t)$ in a dc-component $U_{\pi 1,\rm dc}(t)$, and a first and higher harmonics term $U_{\pi 1,\rm ac}(t)$. The relationship of the higher harmonics to the first harmonic is defined by the nonlinear term $g_{m,nl}$. On taking into consideration that the voltage and the current of the next stage are inverted and shifted as $U_{\pi 2,\rm ac}(t) = -U_{\pi 1,\rm ac}(t-\pi/n\omega)$ and $I_{2,\rm ac}(t) = -I_{1,\rm ac}(t-\pi/n\omega)$, we obtain the following two equations:

$$\begin{aligned} 0 &= \omega^3 R_b^2 C_\mu^2 C_\pi - \omega^2 R_b C_\mu C_\pi \sin(\pi/n) - \omega g_e R_b C_\mu \\ &\quad -\omega\cos(\pi/n)\left(\frac{R_b+R_L}{R_L}\left[C_\mu + C_\pi\right] + C_\mu\left[1+\frac{R_b}{R_\pi}\right] + 2C_\mu\cos(\pi/n)\right) + g_e\sin(\pi/n) \qquad (1) \\ g_{m,nl}\cos(\pi/n) &= g_e - \omega^2 R_b C_\mu C_\pi \qquad (2) \end{aligned}$$

where $g_e = 1/R_L + (R_b+R_L)/R_L R_\pi$. We can find $\omega = \pi/nt_g$ numerically from (1), where $\omega = 2\pi f_{\rm osc}$ and t_g is the gate delay. Moreover, we can determine $g_{m,nl}$ by inserting ω in (2). The first harmonic coefficient b_1 of $U_{\pi 1}(t)$ can approximatively be found from $g_{m,nl}b_1 \approx I_{EE}/2\tanh(b_1/2U_T)$.

Figures 5(a) and (b) show gate delays and voltage swings or first harmonics b_1 respectively for several numbers of inverters n, $R_L = 20\,\Omega$, $I_{EE} = 20\,\rm mA$ and for three cases: (*i*) analytically calculated values, (*ii*) simulated SPICE model (using only the parameters listed in Table 1), and (*iii*) simulated SPICE model of the DHBT. For low numbers of inverters, we see that the gate delay and the voltage swing (resp. the first harmonic) decrease in all three cases. This behavior can be explained by the lack of sufficient time to fully charge all capacitors during the switching event for a low number of inverters. It can be shown that the third and higher order harmonics decrease much faster than the first one and that the voltage swing is almost a sinusoid for low numbers of inverters. Even if the SPICE model of the DHBT splits the base-collector capacitance in inner and outer capacitances and the emitter and collector resistances are neglected in the calculations, the calculated values have an inaccuracy of less than 20% compared to the SPICE simulations.

For a high number of inverters ($n \to \infty$), we can simplify (1) and obtain a formula for calculating the gate delay of a CML inverter:

$$t_{g,\rm CML} = C_\mu R_b + \frac{\frac{R_b+R_L}{R_L}\left[C_\mu + C_\pi\right] + C_\mu\left[3+\frac{R_b}{R_\pi}\right]}{g_e} \qquad (3)$$

On neglecting R_π in (3), because it is very large compared to C_π at oscillation frequencies, and differentiating (3) with respect to R_L, we can obtain an approximation for the load-resistance $R_{L,tg,\min}$ at which the gate delay has a minimum $t_{g,\min,\rm CML}$ for a constant voltage swing V_h: $R_{L,tg,\min} = \sqrt{\tau_f R_b/(4C_\mu + C_{je})}$. For our transistor, we get $R_{L,tg,\min} = 13\,\Omega$. Figure 5(c) shows simulated gate delays for a constant voltage swing $V_h = 400\,\rm mV$ and several load-resistances R_L.

II. Emitter-Coupled Logic (ECL) Inverter

An ECL inverter consists of a CML inverter and an emitter follower (EF, Figure 2) at its outputs. We simplify the large-signal EF model shown in Figure 4 with an ideal output voltage source. We can neglect the base-emitter capacitance C_π for oscillation frequencies below the pole $\omega_{\rm pole} = 1/C_\pi(R_b + R_L)$. For our transistor, this results in an upper limit of $f_{\rm osc} = 20\,\text{GHz}$. The base-collector capacitance of the EF is $C_{\mu,\rm EF} = C_{jc}(0)/(1 + V_h/2\phi_c)^{m_c}$ and the base-collector capacitance of the common-emitter transistor is lower than in the CML case: $C_\mu = C_{jc}(0)/(1 + \phi_e/\phi_c)^{m_c}$ [2]. The result of this analysis with the same approach as for the CML inverter is shown in Figure 5. Calculations predict a decrease of the gate delay and voltage swing (not shown) for low numbers of inverters, while simulations show an increase of the gate delay and that the voltage swing stays almost constant or reduces lightly. The increase of the gate delay can be explained by the increase of the EF-delay ($f_{\rm osc}$ reaches the $\omega_{\rm pole}$ limit). For our transistor, the ECL-gate delay is smaller than the CML one. This is due to two reasons: 1) the base-collector capacitances at dc bias are smaller, and 2) the additional EF-delay is smaller than the decrease of the switching-delay of the common-emitter transistor. This can be explained by the lower output resistance of the EF compared to the common-emitter transistor.

III. Conclusion

For the CML inverter, it has been shown that both gate delay and voltage swing decrease for a low number of inverters due to a lack of sufficient time to fully charge all capacitors during the switching. The presented analytic approximations of the gate delay as a function of the number of inverters show good agreement with the circuit simulations.

Although the voltage swing stays almost constant in an ECL-ring oscillator with a low number of inverters, the gate delay increases due to an augmentation of the propagation delay of the emitter follower for high oscillation frequencies.

Ring oscillators with low numbers of inverters would either underestimate (CML) or lightly overestimate (ECL) the inverter gate delay on measuring the oscillation frequency $f_{\rm osc}$ and subsequently calculating the gate delay as $t_g = 1/(2nf_{\rm osc})$.

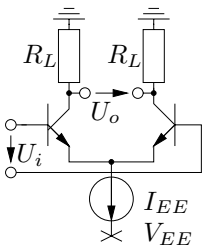

Fig. 1: CML inverter.

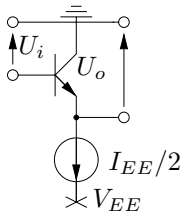

Fig. 2: Emitter follower.

Quantity	SPICE parameter	Value	Units
β	BF	80	
R_b	RB	46	Ω
τ_f	TF	0.72	ps
$C_{je}(0)$	CJE	68.5	fF
ϕ_e	VJE	1.3	V
m_e	MJE	0.22	
$C_{jc}(0)$	CJC	27.6	fF
ϕ_c	VJC	0.1	V
m_c	MJC	0.14	

Table 1: Most important SPICE parameters of the InP-InGaAs DHBT.

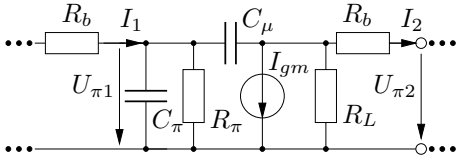

Fig. 3: CML large signal model.

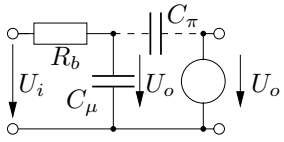

Fig. 4: Emitter follower large signal model.

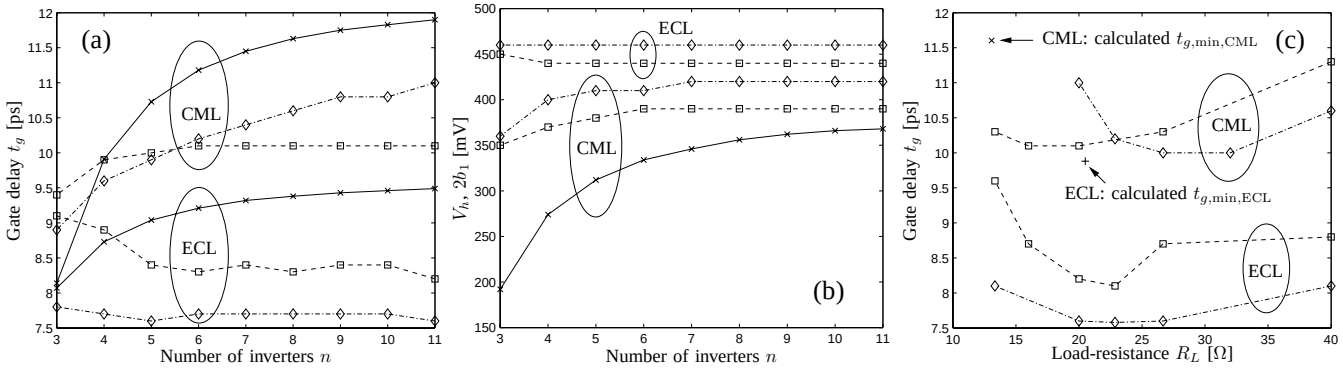

Fig. 5: (a) Analytically calculated and simulated gate delays, (b) voltage swings V_h and analytically calculated, doubled first harmonics $2b_1$, and (c) minimum gate delays for CML and ECL inverters with a constant voltage swing $V_h = 400\,\text{mV}$.
(*i*) Analytically calculated values (solid line, crosses), (*ii*) simulated SPICE model with all parameters listed in Table 1 (dashed line, squares), and (*iii*) simulated SPICE DHBT model (dashed-dotted line, diamonds).

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Organic Thin Film Field-Effect Transistors

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Abstract

In recent years there has been increasing interest in organic materials for fabricating all-organic, flexible, low-cost, and large-area thin film electronics. The standard structure in the development of electronic circuits is the thin film field-effect transistor, with an active "semiconductor" layer, source and drain contact, gate electrode, and a gate dielectric. Each one of these parts is a topic of current research, and some results will be highlighted in the following.

Introduction

When considering the electrical properties of organic materials, one most often associates organic materials with insulators. Rather, organic materials offer a wide range of electrical, as well as mechanical and optical properties. The wide range of physical properties is believed to allow the fabrication of flexible, large-area, all-organic thin film electronics that will find use in current and future electronic applications. The potential for using low-cost manufacturing techniques such as roll-to-roll processing and printing techniques, and the ability to tailor the physical properties of organic materials over a wide range may give organic-based electronics advantages over those based on inorganic semiconductors. Importantly, organic electronics may provide functionality not available with conventional inorganic semiconductors.

For more than 20 years there has been interest in field-effect transistors (FETs) based on thin films of organic semiconductors.[1,2] Organic thin film transistors (OTFTs) are of particular interest for use in sensor, memory, display, and low scale integrated circuit applications. The thin film transistor structure makes use of an active "semiconductor" layer, source and drain contact, a gate dielectric, and a gate electrode, all deposited as thin films and patterned. The active semiconductor layer of the OTFT is a critical part of the device. Two classes of materials are being investigated in depth: polymers ("plastics") and oligomers ("small-molecule" organic molecular crystals). Examples of the first class include e.g. polythiophenes, polyethylenedioxythiophene (Pedot), polyaniline, sulfonated polyaniline, polypyrrole, regioregular poly(3-hexylthiophene). Examples of the second class of materials include pentacene, tetracene, naphthalene, alpha-hexathiophene, C_{60}, and copper-phthalocyanine. Horowitz[3] and Dimitrakopoulos et. al.[4] offer comprehensive reviews of discrete device performance for OTFTs fabricated from many of these materials. For both material classes the macroscopic electronic performance depends in a critical way on the microscopic morphology, in that a higher degree of order leads to a higher charge mobility. While early work on OTFTs of either class of active layer material reveled room temperature field-effect mobility of 10^{-6} - 10^{-3} cm^2/Vs[1,2], significant progress in materials synthesis and processing has been made in recent years leading to significant improvements in performance, with recent reports of OTFTs having mobility of 1-3 cm^2/Vs.[5,6] These values are now considered close to the maximum possible for oligomers[7] and compare favorably with hydrogenated amorphous silicon (a-Si:H).

Similarities and Differences to Inorganic Semiconductors

The microscopic reason for the lower mobility values is closely connected to the nature of the chemical bonding. In silicon the strong covalent bond among Si atoms provides for the chemical and mechanical strength, and the resulting electronic structure is characterized by wide energy bands and a moderate electron-lattice coupling. In contrast, the bonding in organic molecular crystals such as in pentacene, is of van der Waals type and the electronic band width results from the wavefunction overlap between adjacent neutral molecules. As a consequence, the electronic states are strongly affected by any perturbance of the molecular packing and by slightly different packing arrangements

associated with polymorphism. In addition, there is significant electron-lattice interaction and even the best room-temperature mobility (in the range of ~ 1 cm^2/Vs) is at the lower limit for coherent charge transport through band states. In the polymeric semiconductors the charge can move rather efficiently along the backbone of the polymer, but needs to hop or tunnel to the next polymer to travel a macroscopic distance. Again, an ordered polymer network enhances the effective mobility. To date polymeric films with improved molecular ordering and increased field-effect mobility have typically been obtained by using surface aligning layers[8] or by using polymers with side groups that promote self ordering, such as regioregular poly(3-hexylthiophene).[9]

Calling these materials "organic semiconductor" is a slight misnomer, as they are in general intrinsically highly insulating. The controlled introduction of a few mobile charge carriers by doping in the traditional sense is not feasible, as the concept of replacing a few of the neutral molecules in a molecular crystal by "heterovalent" molecules (and fulfilling the stringent steric requirements) is not applicable.

Mobile charges for FET operation need to be injected, requiring a suitable match of the work function of the source and drain electrodes with the relevant electronic levels of the organic semiconductor. Local "doping" of the contact region which is used to form "ohmic contacts to inorganic semiconductors has proven difficult with organic semiconductors. Thus, simplistic energy level diagrams have been used to select source and drain contact metal, aligning the Fermi level (given by the work function) with the relevant carrier transport level of the organic semiconductor (assuming a constant vacuum level). More recently it has been observed by photoemission spectroscopy that contact formation between organic materials and metals is complex and often results in dipole layer formation at the interface which can in some cases result in a significant energy barrier (0.5-1.0 eV).[10] The observed dipole layer formation has been attributed to charge transfer (either with or without contact chemistry) or the modification of the metal workfunction by the organic material.[10] Importantly, the molecular ordering and not surprisingly the electronic structure of the organic film near the contact may also be influenced strongly influenced by the metal surface, further complicating the simple energy level diagram. Most recently, self assembled monolayers have been used to treat the source and drain contact to improve molecular ordering or modify the surface potential of the metal for improved carrier injection.[11,12]

One particular advantageous consequence of the particular electronic structure of organic semiconductors is the absence of unsaturated bonds at the surface and surface states, facilitating the formation of FET structures. However, the film microstructure and not surprising the electrical properties of organic semiconductors deposited on either the insulating substrate or directly on to the gate insulator (depending on device structure) are strongly influenced by the surface conditioning and deposition method.[5,13,14]

Device Parameters and Discrete Device Performance

When evaluating the electrical characteristics of OTFTs, the device parameters most often considered relevant include field-effect mobility, on/off current ratio, sub-threshold slope, and threshold voltage. Of these, the field-effect mobility is often considered the most critical parameter since it sets an upper limit on the switching speed. The maximum operating frequency of a circuit is directly proportional to the field-effect mobility.

For applications such as active matrix displays, a large on/off current ratio is also important. The high intrinsic resistivity of many organic "semiconductors" naturally provides for low "off" (or leakage) current between the source and drain contacts. Low off currents combined with a large field-effect mobility allow for a large on/off current ratio, up to 10^8 for pentacene and 10^6 for a-6T and tetracene.[3,4]

Threshold voltage and sub-threshold slope are particularly relevant to circuit design and determines the operating voltage range. Yet these macroscopic parameters are strongly dependent on microscopic properties, only a few of which are known and understood.

Materials and Device Processing

Discrete devices having been demonstrated for a range of electronic applications. Realization of commercially viable products now critically depends on processing methods. The promise of cost-effectiveness of organic electronics requires the introduction of processing methods that are suitable for the materials, e.g. involve only low temperature steps and require no solvents that are used in traditional lithography. In addition, they should also be applicable to flexible substrates. Of the various approaches, three are mentioned here: micro-contact stamping, ink-jet printing and thermal imaging.

In work by Rogers et. al. the gate electrode, gate insulator, and source and drain contacts have all been patterned sequentially by micro-contact printing prior to the deposition of the organic active layer.[15] More recently Rogers et. al. has demonstrated working OTFTs using stamping techniques to selectively pattern and transfer the organic active layer itself.[16] Using ink-jet printing of soluble organic semiconductors, insulators, and conductors Sirringhaus et. al. have fabricated polymer field-effect transistors and inverters with resistive loads.[8] While ink-jet printing appears to be an excellent method for direct patterning of soluble organic semiconductors, the patterning of small-molecule organic semiconductors remains a challenge. To date the highest mobility small-molecule OTFTs have been fabricated by vacuum subliming thin films of organic semiconductors onto carefully prepared surfaces using well-controlled deposition conditions. Thermal imaging appears to be an attractive technique for selectively depositing small-molecule organic semiconductors.[17] All three techniques have tremendous potential and it is likely more processing techniques will be developed given the wide range of physical properties offered by organic materials.

It is worth noting that the choice of materials or processing technique usually restricts the choice of the other. Thus careful consideration must be given to materials integration and processing. Importantly, the choice of materials and processing in many cases also restricts the choice of device architecture. Several device structures have been investigated, however planar structures similar to the staggered-inverted structure typically used for fabricating a-Si:H TFTs have been most extensively studied. More recently, there have been attempts to fabricate sub-micron channel length vertical device structures.[18]

Circuit and Display Demonstrations

In the past few years, many of the individual steps have been combined to produce first demonstration circuits that have brought “plastic electronics” in the headlines of the popular press. So far they all are single items from the laboratory bench, yet they reveal many of the intriguing aspects of “plastic electronics”. For instance, about five years ago all-polymer integrated circuits have been produced on flexible polyimide substrates, including a 15-bit programmable code generator which operated at 30 bits/s.[19] Soon circuit speed was increased to 100 bits/s for such devices.[20] Ring oscillator circuits reported on around that same time which were based on the small-molecule organic semiconductor pentacene and fabricated on rigid substrates had single propagation delays of as low as 75 μs,[21] and integrated organic (pentacene)/ inorganic (a-Si:H) complementary circuits on rigid substrates were also reported with single stage propagation delays as low as 5 μs.[22] The scale of integration further increased, with complementary organic circuits comprised of nearly 1000 complementary elements (integrated n- and p-channel OTFTs) to form a 48-stage shift register clocked at 1 kHz.[23] More recently ring-oscillator circuitry based on soluble polymers for both the active and the insulating layer has been demonstrated, operating with single stage propagation delays of 0.7 μs[24] and ring-oscillator circuitry based on vacuum sublimed pentacene as the active and a solution processable polymer as the insulating layer, operating with single stage propagation delays of 22 μs.[5]

Combining flexible organic circuits with flexible displays appears particularly interesting for current and future display applications. Of the more recent demonstrations a few examples are mentioned here: a monolithic integrated polymer-dispersed liquid crystal display driven by organic thin film

transistors produced by rubber-stamping[25] or conventional photolithographic patterning[26] on flexible polymeric substrates. A circuit consisting of 4096 solution-processed polymeric transistors has been used also as driver for a 2-inch active-matrix display on glass substrate operating at video speeds and at 256 gray levels.[27]

Conclusion

There has been tremendous progress in OTFT performance in recent years. Despite recent advances and impressive laboratory scale demonstrations, considerable challenges remain. Importantly, the development of low-cost, high through-put deposition and patterning techniques for fabricating devices with sub-millimeter features is critical to the commercialization of organic-based electronics. And while not discussed here in detail the synthesis and integration of electrically stable organic materials is equally critical, as long term operational stability remains a concern. Consequently, the promise of low-cost ubiquitous electronics and the continued improvement in device and circuit performance, despite a relatively limited understanding of the physical properties of organic materials, make organic electronics a topic of considerable commercial and scientific interest.

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A FECTED for Low Voltage Operation

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While the FECTED is still an interesting microwave source, one of it's drawbacks has been the high operation voltage required. By employing a new type of anode contact we have been able to lower this voltage substantially thereby making the FECTED more suitable for portable operation and improving it's reliability.

Introduction

The FECTED (**F**ield **E**ffect **C**ontrolled **T**ransferred **E**lectron **D**evice) has been an attractive signal source at millimeter wave frequencies for many years. A remaining severe drawback of the device is its high supply voltage, typically between 7 V and 8 V making its use in battery powered units problematic. In addition to making portable operation easier a reduction of the supply voltage also reduces the field strength in the device, thereby reducing the risk of breakdown and improving the reliability of the FECTED.

Design

Figure 1 shows a cross-sectional view of the modiefied FECTED-structure investigated in this work. While the cathode (source) configuration, consisting of an ohmic contact and an overlapping Schottky contact, is identical to that of the standard FECTED and HEIFET (e. g. [1], [2], [3], and [4]), now the same contact structure is also employed at the anode (drain) side. Although the contact structures are identical, the Schottky contacts at the anode and the cathode serve different purposes. The task of the Schottky source is to generate a depleted region in the underlying channel, thereby accelerating the electrons injected by the ohmic source until a stationary Gunn domain has formed there. The idea behind the combined drain contact is to overcome the particular drawbacks of either the ohmic or the Schottky contact. In the case of an ohmic drain, the sharp increase in the electric field in the neighborhood of the contact is problematic and is a common reason for device failure. If on the other hand a conventional Schottky contact is used, a voltage drop in the order of 0.8 V has to be accepted across the contact. Using a combination of both contacts gives an additional degree of freedom by separately adjusting the bias voltages applied to the Schottky drain and the ohmic drain in such a manner that the total electric field is kept uniform in this region. RF–wise the drain contact structure acts as a single electrode due to the thin SiO_2 layer coupling the Schottky drain to the ohmic drain contact.

Experimental Verification

First prototypes of the new FECTED with an on-chip oscillator circuit have been manufactured at the cleanroom of the *Microelectronics Institute*. Figure 2 shows the output power of

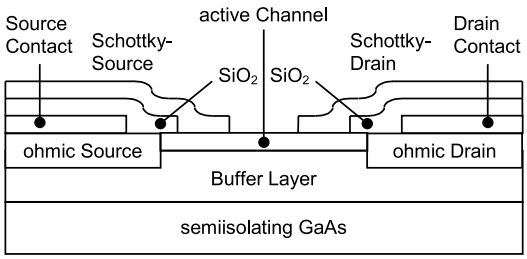

Figure 1: Cross-sectional view of the new FECTED-structure

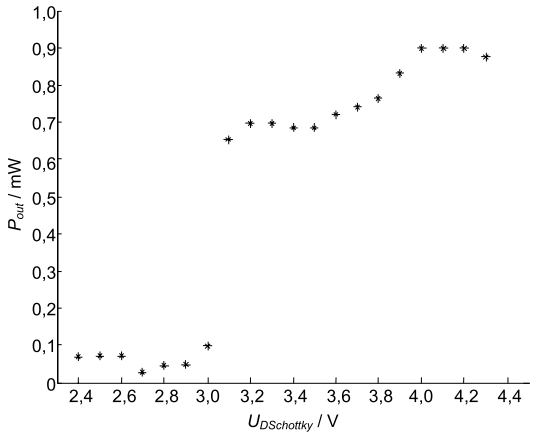

Figure 2: Measured output power of a prototype of the new FECTED-structure

the device at the resonating frequency of 58 GHz as a function of the voltage $U_{DSchottky}$ applied to the Schottky drain. The bias voltage applied to the Schottky source was $U_{SSchottky} = -2\,\mathrm{V}$, the ohmic drain was biased at $U_D = 3\,\mathrm{V}$, and the ohmic source was kept at $U_S = 0\,\mathrm{V}$ (ground). As can be seen in Figure 2, significant output power is generated if $U_{DSchottky} \geq U_D$. The efficiency of the oscillator is still low ($\eta \simeq 0.3\%$) but we are confident that it can be improved significantly by optimizing the oscillator circuit.

Conclusion

A FECTED for low voltage operation at high microwave frequencies has been fabricated and tested. The device seems to be well suited for use in the 61 GHz ISM band which will be of increasing commercial interest in the years to come. While the output power around 1 mW is sufficient for near range applications, the authors believe that power as well as efficiency can be significantly improved by optimizing the oscillator circuit.

Acknowledgments

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Nanoimprinted GaInAs/InP Circuits Based on Three-Terminal Ballistic Junction Devices

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We used nanoimprint lithography (NIL) for fabrication of circuits with three-terminal ballistic junction (TBJ) devices and quantum point contacts (QPC) in a GaInAs/InP high mobility two-dimensional electron gas (2DEG). The TBJ-devices and QPCs are interconnected to realize logic elements, e.g. "AND" and inverter circuits. The fabrication process includes a NIL imprint in PMMA resist, oxygen plasma ashing of resist residues and wet etching of GaInAs/InP to form the TBJ-devices, QPCs and leads. Features as small as 150 nm in GaInAs/InP can be reproducibly fabricated in a direct nanoimprint step. Functionality of NIL-made devices is demonstrated.

A new nanoelectronic device, three-terminal ballistic junction (TBJ) device [1] can be modeled as three quantum point contacts (QPC), coupled via a ballistic cavity. Because of its design, a TBJ-device shows non-linear electrical characteristics [1,2], which can be used in a variety of nanoelectronic logic applications or frequency multiplication [3,4]. The TBJ-structures with characteristic size of 100-200 nm can easily be implemented in GaInAs/InP or GaAlAs/GaAs using electron beam lithography (EBL) and wet etching [2,3,4]. Recently we have demonstrated a functioning TBJ-device in GaInAs/InP with ≈100 nm features using nanoimprint lithography (NIL) [5]. Here, we present the NIL-based technology for making the TBJ nanoelectronic logic circuits in GaInAs/InP 2DEG high mobility material.

For fabrication of the TBJ and QPC devices, we used a high mobility $Ga_{0.25}In_{0.75}As$/InP 2DEG heterostructure with electron concentration of $4.5x10^{11}$ cm^{-2} and mobility 1.2 m^2/Vs at room temperature. The 2DEG is confined in $Ga_{0.25}In_{0.75}As$ quantum well (QW) positioned 50 nm below the surface. The electrons are supplied to the QW from a 2 nm thick delta-doped (Si) InP layer placed 20 nm above the 2DEG. The stamp for the NIL was made from a one-inch, thermally oxidized SiO_2/Si wafer. The wafers were patterned using electron beam lithography, Cr lift-off and reactive ion etching of SiO_2. A variety of patterns, consisting of TBJ-devices and QPCs were exposed on the stamp wafer. Using Cr layer as an etching mask in reactive ion etching, silicon oxide was etched to a depth of about 100 nm. For the NIL experiments, a GaInAs/InP sample was spin-coated with ≈120 nm thick PMMA resist (950 kDa) and imprinted for 3 min at 50 bar and T=200°C. After release of the stamp, resist residues were removed in an oxygen plasma. Wet chemical etching was used to etch about 70 nm of GaInAs/InP material to form the active devices. Fig. 1 shows imprinted and etched test GaInAs/InP circuit, which consists of two TBJ-devices and one QPC, with respective side gates. In order to test the functionality of the fabricated devices, one of TBJ-structures was characterized electrically. Voltages V_L and V_R were applied to the left and right branches, respectively, and potential V_C was measured as a function of voltage V_0 ($V_0=V_L=-V_R$), Fig. 2 (a). Application of voltages in a push-pull mode resulted in a parabolic dependence of V_C vs. V_0, as predicted by theory. Similar dependence was observed also in TBJ-devices patterned by EBL [2]. Fig. 2 (b) shows such parabolic behavior of voltage on a stem electrode V_C as a function of V_L for a NIL-made TBJ-device at room temperature. It has been shown theoretically [6] that a non-linear characteristic of the TBJ-devices can be used for realization of logic functions. A logic circuit "AND", for example, can be implemented in the following way. When high positive voltages V_L and V_R (logic value 1) are applied to both left and right input of the TBJ, the output voltage V_C will be positive (logic value 1). Otherwise, the output voltage will be low (logic value 0). The QPC is used as a load for the "AND" gate, see Fig. 2(a). The electrical characterization of the NIL-made logic circuits is under way.

Acknowledgements
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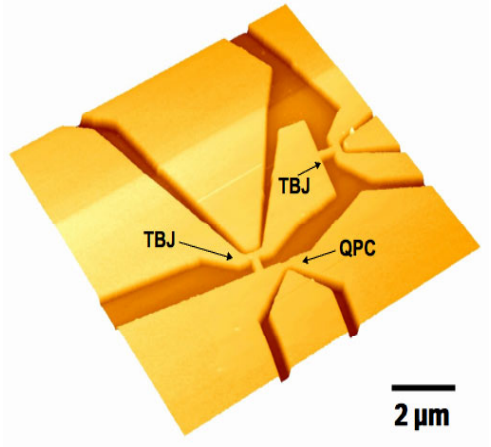

Fig. 1. AFM image of imprinted and etched test GaInAs/InP circuit. The circuit consists of two TBJ-devices and one QPC. The features of the devices are about 150 nm.

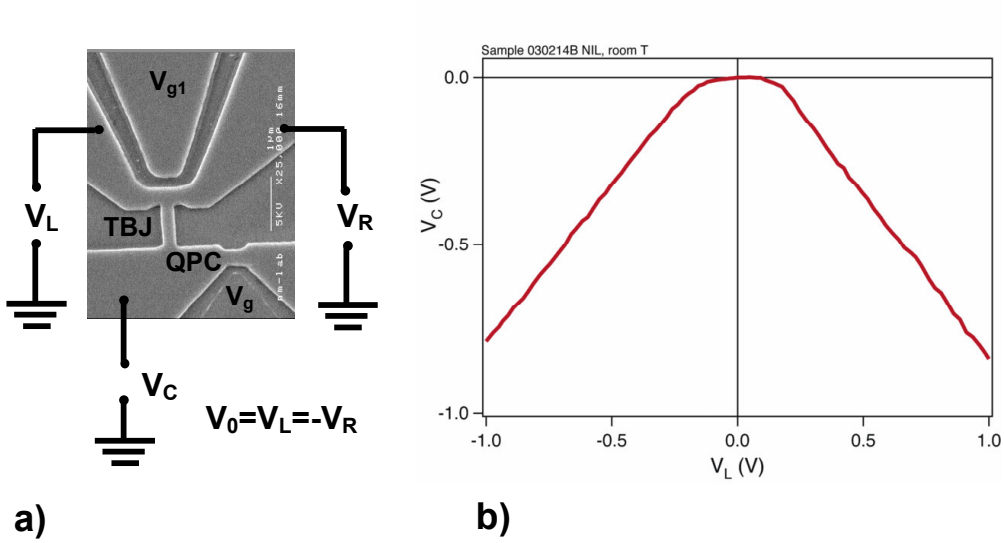

Fig. 2. (a) Schematic illustration of a test measurement of NIL-made TBJ-device. The QPC serves as a load for the TBJ-"AND" gate. (b) Room temperature functional test measurement of the NIL-made TBJ-device. For low V_L, voltage on central (stem) electrode (V_c) depends parabolically as a function of V_L, with $V_0=V_L=-V_R$, as predicted by theory [1]. The TBJ-devices made using nanoimprint, show similar nonlinear characteristics as the TBJ-structures patterned with EBL, indication absence of a NIL-related damage.

Tunnel Schottky contacts with 2D channel, a new mechanism of negative differential conductance

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A mechanism of inherent negative differential conductance (NDC) in tunnelling from a metal into 2D subband in a quantum well is proposed. The NDC due to the mechanism should be observable in the specially designed structures similar to the "inverted" HEMT. The I-V curve for the tunnel current between the gate and 2D channel in such structures should have the N-type form with NDC region. An example of Al/delta-doped GaAs/AlGaAs structure is considered and theoretical tunnel characteristics will be presented. NDC is a consequence of the Schottky barrier height increase with bias for the electrons tunnelling resonantly into the 2D subband. An extremely fast nature of the tunnelling processes let me believe that the kind of structures could be of interest for high-frequency applications.

Introduction

Tunnelling is a very fast process, e.g., it has been demonstrated that the resonant-tunnelling diodes (RTDs) can work up to the frequency of 3.9 THz [1]. In combination with the negative differential conductance (NDC), as in RTD, that gives possibility to realize oscillators and sources of radiation at very high (for electronics) frequencies, e.g., the oscillator based on RTD has been demonstrated at 712 GHz [2]. That is why the semiconductor tunnel structures with NDC attract a lot of attention. In the existing semiconductor tunnel structures the NDC appears due to the abrupt band edges in the electronic band structure of the devices. In RTD, the NDC appears when the abrupt conduction band bottom in the emitter becomes higher than the bottom of the 2D subband in the quantum well (QW). In the Esaki diode, the NDC arises when the abrupt conduction band bottom on the emitter side becomes higher than the top of the valence band on the collector side. The novelty of the mechanism considered in the present work [3] is that the abrupt band-edges are irrelevant – the electrons tunnel from the metal where the band edges are very far from the Fermi level – the NDC appears solely due to the deformation of the Schottky barrier with bias.

NDC mechanism

Let us consider a structure where the metal is separated from a narrow QW by a triangular Schottky barrier. The QW is formed by the Schottky barrier on one side and the heterobarrier on another one. An example *Al/δ*-doped *GaAs/AlGaAs* structure is shown in Fig.1. The ground 2D subband (E_0) in the QW is filled by electrons due to δ-n-doping near the *GaAs/AlGaAs* heterointerface. The whole structure is slightly p-doped, that confines the electrons to the QW. The δ-n-doping level in the QW is chosen in such a way that the QW is conducting along the well, but the Fermi level is significantly lower than the bottom of the first excited 2D subband (E_1). The lateral contacts to the 2D electron channel (QW) should be fabricated in the same way the drain and source contacts are made in the HEMTs. Both two- and three-terminal structures could be realized in such a way.

The mechanism of the NDC is the following. Let's apply a (positive) bias between the metal and 2D channel so that electrons tunnel from the metal to the empty states in the QW between the Fermi levels in the metal (μ_m) and semiconductor (μ_s), $\mu_m > \mu_s$. The tunnel current (J) is: $J \propto T(\mu_m - \mu_s)$, where T is the tunnel transparency of the triangular barrier for electrons tunnelling into the ground 2D subband in the QW. With small increase of bias ($\delta\mu_m$), the tunnel current changes due to two contributions: $\delta J \propto T\delta\mu_m + (\mu_m - \mu_s)\delta T$. First, the number of empty states between μ_m and μ_s increases. The contribution is positive and proportional to $T\delta\mu_m$. Second, the tunnel barrier becomes higher for the electrons tunnelling into E_0 subband

and T decreases ($\delta T<0$). The contribution is negative and proportional to applied bias: $(\mu_m-\mu_s)$. At low biases the first contribution is the dominant one, at higher biases the second contribution increases as $(\mu_m-\mu_s)$ and becomes larger than the first one. J starts to decrease in that case and NDC appears on the I-V curve, e.g., that happens at the bias of approximately 60mV in the example structure in Fig.1, see Fig. 2.

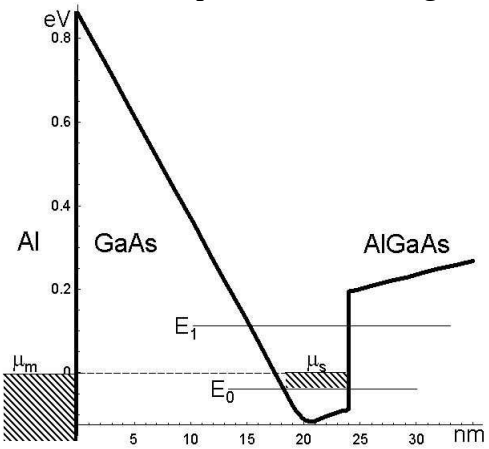

Fig.1: The conduction band profile of $Al/GaAs/Al_{0.3}Ga_{0.7}As$ structure calculated selfconsistently. The thickness of the GaAs layer is 24 nm, the whole structure is slightly p-doped with $N_p=10^{16}\ cm^{-3}$ and there is δ-n-doping with $N_n=5\cdot10^{12}\ cm^{-2}$ 20 nm below $Al/GaAs$ interface. The electron concentration in the QW is $1.1\cdot10^{12}cm^{-2}$.

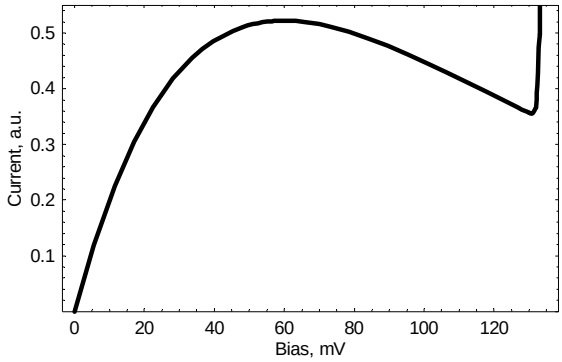

Fig.2: The I-V curve between the *Al* gate and 2D channel of the structure shown in Fig.1.

The tunnelling to the higher subbands (e.g., E_1) increases the tunnel current and the NDC disappears. So, the QW should be narrow enough to keep the bottom of E_1 subband sufficiently high, e.g., $E_1-\mu_s\approx120\ meV$ and the NDC should be observed between *60* and *130 mV* (E_1 gets a bit higher with bias) in the example structure in Fig.1. In the standard HEMT structures, the barrier is made of wide-bandgap semiconductor, i.e., the sequence of wide- and narrow-bandgap layers is opposite to that in Fig.1, so proposed structure is similar to "inverted" HEMT. In ordinary HEMTs, the electrons in the QW are confined by a slowly increasing (due to p-doping) potential on the right-hand side. Therefore, the QW is wide and the 2D-subband separation (E_1-E_0) is not sufficient to achieve NDC.

The structures similar to the one proposed in the present work, but without heterointerface, have been studied experimentally before [4]. The QW is also wide in the case, $E_1-E_0\approx50\ meV$, which is not enough the NDC to appear.

In principle, the δ-n-doping could be made outside the QW, so that it does not degrade the electron mobility along the QW. In such a way a HEMT with NDC between the gate and channel can be realized.

Acknowledgements

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Left handed material–based transmission lines in a waveguide technology

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We report on the study on an electromagnetic left-handed waveguide based on double negative material systems. The negative permittivity is achieved via the cut-off of the waveguide whereas the negative permeability is obtained through split ring resonators. The formation of a transmission window is demonstrated under the condition of simultaneous negative permittivity and permeability from full wave analysis of the EM behaviour of the system which are favourably compared to the recent measurements carried out for this system *PRL Vol. 89, p. 13901,October 2002*)

Left handed material systems are now attracting much interest after the demonstration of a pass band when the propagation medium exhibits negative permittivity and permeability simultaneously [1]. This was possible owing to the proposal of Pendry of using non magnetic Split Ring Resonators (SRR's) [2] for negative permeability and thin wires for negative permittivity. Under these conditions, it can be shown that the phase and Poynting vectors are anti-parallel. These media were called Left handed materials (LHM's) by Veselago about three decades ago [3]. So far most of the studies devoted to this topic addressed free-space prototypes constituted of imbricate arrays of thin wires and SSR's highlighting the bulk material properties by de-embedding notably the permittivity and permeability values from the transmission and reflection coefficient. Recently however a number of studies have focused on transmission lines either by lumped L-C circuit in a high pass mode [4] or in a waveguide technology [5]. In this paper, we addressed the latter approach by taking advantage of the cut-off effect of a waveguide in order to achieve a negative permittivity medium while the negative permeability is obtained via an array of SRR's placed in the E-plane. By this means, it is shown the possibility to recover a transmission window with an expected backward propagation behaviour whose bandwidth is closely related to the coupling between the lumped resonators and their number. Instead of a true mini-band, as it will be the case for infinite media, the device exhibits a discrete set of very high quality factor transmission peaks. We are discussing these results in the context of practical applications making use of such LHM's for which the insertion loss are of prime importance.

Figure 1 shows a schematic of the half of the propagation structure aimed at operating around 6 GHz. It consists of a waveguide section below the cut-off namely with sub-wavelength dimensions ($d < \lambda$). A rectangular waveguide such as those used for communication can be used but for sake of simplicity here we chose a square metallic shield as in [5]. Feeding to the structures is achieved by means of two coaxial–type probes. Under this condition, the magnetic field is correctly oriented with respect to the array of metallic SRR's patterned on a dielectric substrate. The overall planar circuit is composed of various resonators (in the present example three) tightly coupled in the propagation direction. Another particularity of metamaterials is the fact that their relevant dimensions are much shorter than the wavelength. For the device depicted in Fig. 1 the cut off of the central waveguide ($\lambda/2$ condition) would be 25 GHz. As a consequence for an operating frequency of 6 GHz, as demonstrated below, we are in a long wavelength regime satisfaying the aforementioned criterium. Also with respect to an array operating in free space which is constituted of a very high number of printed board SRR's it can be shown that we take advantage of image effect due to the metal shielding surrounding the SRR array. Clearly one of the drawback of this scheme is the difficulty to feed the planar structure. To face this difficulty and hence to improve the evanescent coupling between the full and shrunk waveguides the dielectric plates have been slightly inserted through the input and output waveguides.

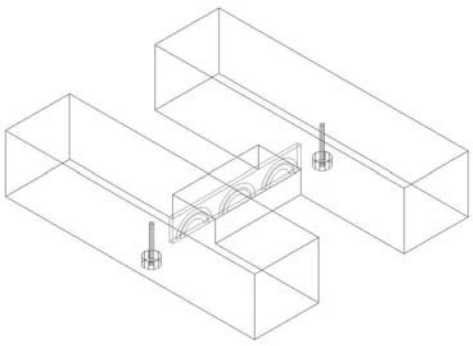

Fig. 1 Schematic of the LHM based waveguiding section

Full wave electromagnetic analysis was carried out by means of the computation of transmission and reflection coefficients from port-to-port equivalent to the elements of the symmetric scattering matrix Sij. 3-D Maxwell equations were solved in the frequency domain by finite element method. There is no special care paid to the metal shield which acts as a perfect electric field

boundary making some image replica in the directions normal to the propagation direction.

Figure 2 shows the frequency dependence of scattering parameters (Sij) we calculated using the dimensions of the structure characterized in [7]. Finite thickness for the metal was included but the metal losses were neglected with an infinite conductivity. Ab initio computation of the frequency response of SRR have shown a resonant in the targeted frequency range with a central frequency around 6 GHz.

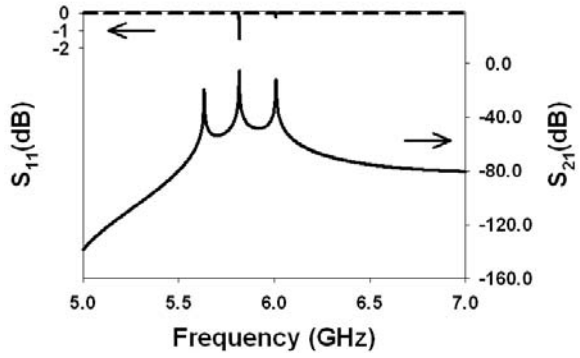

Fig. 2 Frequency dependence of scattering parameter S_{21}

Figure 3 is a close up of the resonant transmission which approaches 0 dB. The bandwidth defined by the edge peak is of about 0.4 GHz due to a strong coupling effect in the propagation direction.

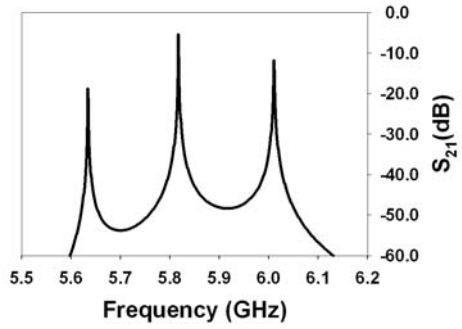

Fig . 3: illustration of the quality of the resonance for a 3-SRR device

Figure 4 shows the mapping of electric field in the SRR plane. It can be noticed that the field accumulated as expected around the metallisation. Therefore it was not, a priori, necessary to concentrate the field by means for instance of a fin line technology [6]. It can be emphasized however that in this latter technology it could be simpler to couple the energy with a circuit patterned with sequential rings and wires in order to meet the requirement of negative permittivity and permeability in a full size waveguide. Figure 5 displayed the variations of the scattering parameter S_{21} for a 9-SSR waveguide structure. 9 peaks, according to the number of resonators, are apparent in the frequency dependence of S_{21}. The key result is the fact that the resonances are very sharp so that in practice the average level is extremely low around 30 dB as found from the measurements [8].

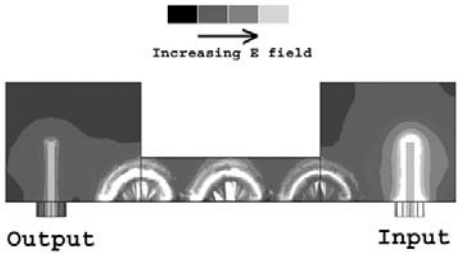

Fig. 4 Electric field mapping in the SRR plane

This means that the losses are due to a quasi localization with long life time (high Q) and not, as sometimes evocated, to metal losses. On the other hand the bandwidth, except the last peak with a frequency shift not explained so far, is roughly conserved as it will be the case for electric networks or electronic superlattices.

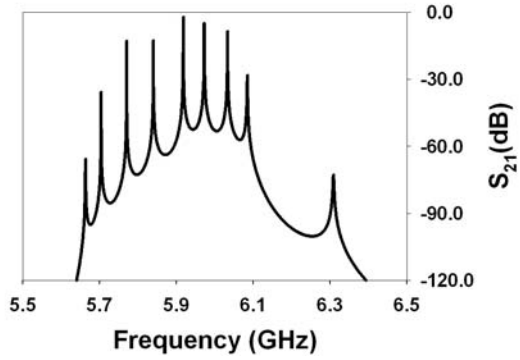

Fig. 5: variation of the matrix element S21 as a function of frequency for a 9-SRR section

In conclusion, we have analysed by a full wave analysis of a metamaterial-based waveguide system. It is shown that the average level is low due to high Q factor resonances characteristic of electromagnetic localisation in the multiple resonators.

Acknowledgments

The authors would like to thank R. Marques and his collaborators for sending their experimental results and for fruitful discussions.

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TERAHERTZ TECHNOLOGY

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ABSTRACT As we begin the new millennium, significant scientific and technical challenges remain within the terahertz (THz) frequency regime and they have recently motivated an array of new research activities. Indeed, the last research frontier in high-frequency electronics now lies in the so-called *terahertz* (or submillimeter-wave) regime between the traditional microwave and the infrared domains. During the last few years, major research programs have emerged within the U.S. Army and the U.S. Department of Defense (DoD) that have been focused on advancing the state-of-the-art in THz-frequency electronic technology and on investigating novel applications of THz-frequency sensing. One of the main catalysts for these programs is associated with the idea of using the fundamental interactions of THz radiation at the molecular level for sensing and characterizing chemical and biological (CB) agents. While new research indicates there are potential payoffs in this application area, both to the military and private sector, the existing technological challenges to fielding robust, compact and cost effective components remains formidable. To this end, the U.S. Army Research Office (ARO) is actively promoting fundamental research in THz technology within its Solid-State & High Frequency Electronics Program. This paper presents an overview of these projects that seek to field a future THz Electronics capability.

I. INTRODUCTION

Today, the *terahertz* or *THz* regime has been broadly defined as the portion of the submillimeter-wavelength electromagnetic (EM) spectrum between approximately 1 mm (300 GHz) and 100 μm (3 THz). While the THz frequency regime has long offered many important technical advantages (e.g., wider bandwidth, improved spatial resolution, component compactness) and while significant scientific interest in THz frequency science and technology has existed since the early 1900's, the solid-state electronics capability at THz frequencies today remains extremely limited from a basic signal source and systems perspective (i.e., the best output power is less than or on the order of milliwatts). Two-terminal transport-based semiconductor devices long ago emerged as the key technology for the generation, amplification and detection of electrical signals at submillimeter-wave frequencies. However, the overall performance (e.g., power and efficiency) of even state-of-the-art two-terminal technologies suffers as they are extended for operation high into the THz band. This longstanding limitation in THz electronic technology, along with the excessive cost of instrumentation, has certainly been a major stumbling block to new scientific inquiries at THz frequencies and has most probably prevented the spread of science and technology related issues to the broader scientific and engineering communities. The growing interest in the precise detection, identification and characterization of very small organic and inorganic systems has already begun to emphasize the future value of a robust THz-frequency sensing science and to establish it as an important driver for the rapid advancement of electronics technology at THz frequency. These new and exciting sensing applications only provide added motivation for realizing a practically useful THz electronics technology, which has long been recognized to offer much to conventional electronic application areas such as extended bandwidth for special scenario communications (i.e., short-range, networked and satellite) and significantly enhanced signal processing power. Historically, the U.S. DoD has been instrumental in establishing the basic foundations for many important endeavors in science and engineering and recent DoD support for THz electronics is once again playing a major role in promoting an interest among the broader community. Indeed, there has been a steadily growing interest among the international scientific and technical communities in the unique challenges associated with developing a robust electronics technology and with developing a detailed understanding of THz-frequency sensing science [1]. The U.S. ARO currently supports an array of research activities in the THz technology. These projects are addressing the future needs in THz-frequency solid-state electronics through (i) Advanced

Device Engineering, (ii) Advanced Systems Development, and (iii) Innovative Device Concepts. These efforts span the electronic and photonic regime and will be discussed in the sections that follow.

II. ADVANCED DEVICE ENGINEERING

The detection and identification of chemical and biological (CB) warfare agents is definitely a high priority to the U.S. military Joint Service's CB defense mission. As the potential for the detection and discrimination of CB materials using THz technology has been previously demonstrated by collaborative research programs [2] between the U.S. ARL and the U.S. Army Soldier Biological and Chemical Command (SBCCOM), ARO has developed research programs that seek to achieve significant engineering advances in traditional device technology that has already demonstrated utility at THz frequencies. For example over the last few years, support from a DoD Multi-disciplinary University Research Initiative (MURI) and Small Business Innovative Research (SBIR) has been implemented by ARO to support the development of "Semiconductor-Based, Fully-Integrated, Terahertz, Transmit/Receive (T/R) Modules," using Schottky diode and heterostructure barrier varactors (HBV's) device technology. The goal of this collaborative research effort between the University of Virginia (UVA) and Virginia Diodes, Inc. (VBI) is to demonstrated T/R technology that is suitable for military applications. Here, compact, reliable and cost effective components are being developed through innovations in high-level integration that is achieved through the use of advanced diode fabrication processes and extensive reliance on advanced computer aided design and simulation tools. The advanced GaAs-on-dielectric fabrication process used for these circuits (see Fig. 1) facilitates the integration of diodes with other components which reduces parasitic effects and leads to greater efficiency, sensitivity and bandwidth. This high precision integration also allows for advanced design and optimization and eliminates much of the hand soldering which in turn improves reliability. Advanced engineering techniques were applied under the Phase I SBIR effort to develop diode-based architectures with remarkable T/R component performance (e.g., 200 GHz receiver with unprecedented sensitivity and bandwidth, tripler design with full waveguide bandwidth at 300 GHz, 200 GHz transmitter with 100 mW of power), however, the primary significance of the new prototypes was their unprecedented convenience. They are compact and reliable, use no mechanical tuners, require no dc bias and are exceptionally easy to manufacture. Under Phase II, significant accomplishments have already been made in the areas of heterodyne receivers, broadband transmitters, high power transmitters, and in fabrication technology. For example, a state-of-the-art 600 GHz integrated mixer circuit was developed with excellent performance (mixer noise temperature of 1,540 K, a mixer conversion loss of 7.9 dB, a local oscillator power requirement of 3.4 mw (@ 300 GHz) and a system noise temperature of 2,920 K). Note this is the best noise temperature ever achieved with a subharmonically pumped mixer in this frequency band and it is very easy to assemble. Significant progress has also been achieved on a whole array of broadband doublers, triplers and quintuplers which targets a long-term goal of 600 GHz T/R components. For example, recent efforts were dedicated to design, built and tested a high-power version of a broadband tripler design and were used to successfully cascaded this device with a second stage broadband tripler.

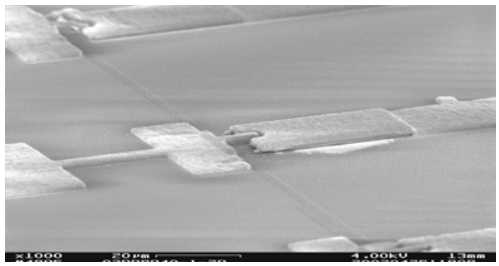

Fig. 1. *A GaAs-on-quartz integrated diode.*

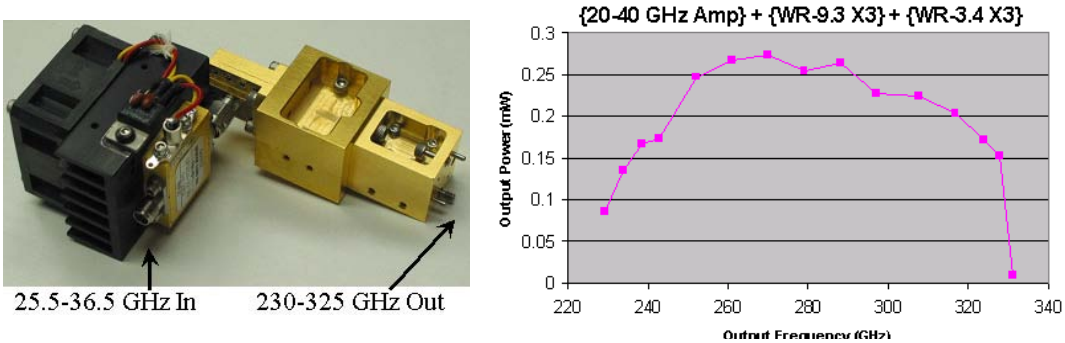

Fig. 2. *The performance of a cascaded tripler-tripler chain to 230-325 GHz. The input drive power is less than 1 mW in the band from 25.5-36.5 GHz. No tuners and the source signal may be swept to any frequency in the band.*

The initial results of these tests are given in Fig. 2 along with a photograph of the actual amplifier/multiplier chain. This design achieved greater than 200 μW from 245-315 GHz and greater than 50 μW from 230-325 GHz in this x9 multiplier chain. It is important to note that the ARO also supports device engineering research in other more high-risk areas to address such issues increased power and efficiency future systems. These areas include a Plasma-Wave electronic device (RPI), a Ballistic Tunneling Transit-Time device (U. of Michigan), an Ultra-wideband Photomixer Source (UCLA) and a Coupled Asymmetric Quantum Dot Laser device (Stanford University). Each of these concepts represents well-established device concepts that require specific engineering extensions/improvements to realize THz frequency operation and these aspects will be overviewed in the oral presentation.

III. ADVANCED SYSTEM DEVELOPMENT

In the past decade, there has been a proliferation of chemical and biological (CB) agents as instruments of warfare and terrorism. Therefore, it is not surprising that the issue of establishing an automatic detection, alert, avoidance and protection systems for areas contaminated by weapons of mass destruction is a high priority within the U.S. DoD. The existing limitations in the point-detection and standoff (i.e., remote) sensing of chemical and biological warfare agents motivate an assessment of the effectiveness of THz spectroscopic and imaging techniques towards these goals. For example, ARO currently supports multiple efforts (i.e., through core, MURI and the Small Business Technology Transfer (STTR)) that seek to design, build and field-test a THz-frequency differential-absorption spectrometer that can be used for the remote detection of biological warfare agents. This envisioned sensor system is being developed such that it is deployable both as a stationary perimeter defense system and as an outward-looking remote scanning system. The foundation for these efforts was established through collaborative research efforts between ARL, SBCCOM, UCLA and UVA [3]. Here, design studies were conducted for a differential-absorption-radar (DAR) approach that utilizes the spectral signatures of *Bacillus (B.) Subtillus* spores within the THz regime as the detection mechanism. These studies considered DAR remote sensing of biological (bio) clouds at significant ranges (i.e., 1 km) and include the effects of realistic atmospheric conditions. A high-level remote-sensor design was used to estimate the probabilities of detection (p_d) and false-alarm (p_{fa}) associated with this general technique. These studies suggest useful remote-detection performance can be achieved (i.e., $p_d > 0.9$ & $p_{fa} << 10^{-4}$ for bio-cloud densities < 10^3 cm^{-3}) at 1 km ranges if the THz signature information remains predictably stable under varying atmospheric conditions (e.g., changes in humidity, spore activity state, etc). Furthermore, a realistic bio-agent airframe attack scenario was utilized to demonstrate standoff detection of bio-clouds with ~100% confidence while outside the threat-level concentrations. Fig. 3 (a) depicts one bio-agent scenario considered where 1 kilogram of material is

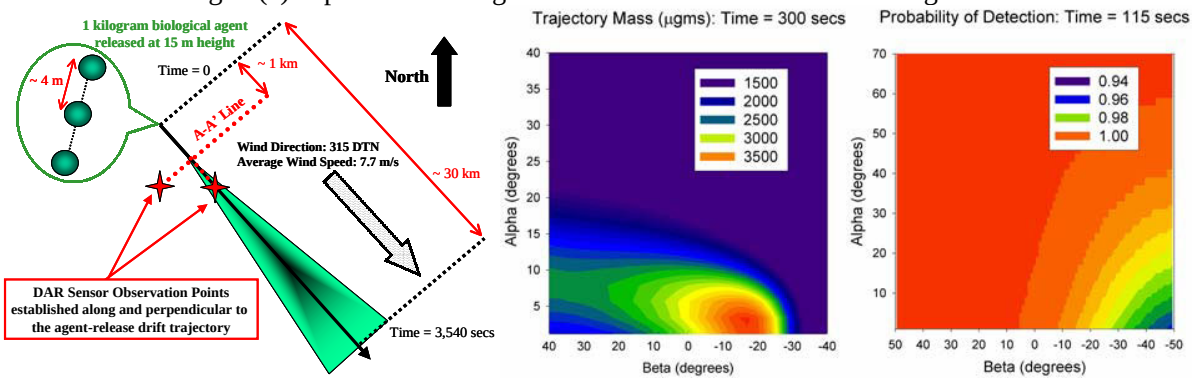

Fig. 3. *(a) bio-agent release scenario, (b) trajectory mass, and (c) pd of cloud, of cloud from downwind.*

released and drifts over a 30 km range. Imaging studies were performed from observer positions perpendicular (A'-A line) to and along the cloud drift region. Fig. 3 (b) gives an image of the trajectory mass (i.e., the bio-particle mass within a cylinder of aperture 1 m^2 along the DAR sensing trajectory) of the cloud along the A'-A and 300 s after the release. Fig. 3 (c) gives a mapping of the p_d from a position along the release trajectory. These, and other images, have been used to determine that 100% confidence in remote detection can be achieved while the bio-concentration remains significantly below threat levels (i.e. < 0.6 cm-3). These results suggest standoff capability is feasible for threat-level concentrations in

practical battlefield environments at sufficient ranges to provide for early warning. ARO also manages a number of other system development programs [4] including efforts for; implementing a Fast Scan Submillimeter Spectroscopy Technique (FASSST) using existing solid-state technology (Ohio St.), extending T-Ray to image large targets at remote distances (RPI), achieving THz-based characterization of nano-engineered artificial dielectrics (NJIT), and for developing THz Interferometric Imaging Systems (TIIS) for Detection of Weapons and Explosives (Picotronix).

IV. INNOVATIVE DEVICE CONCEPTS

While outstanding progress has been made in the area of THz electronics, significant challenges remain for realizing compact, cost effective and robust device components. In an effort to provide innovative device concepts for the future, ARO supports a number of high-risk projects that seek to discovery new high-frequency source concepts that have the potential for increases to output power and efficiency. For example, the U.S. ARL-ARO has a collaborative research effort that is establishing engineering criterion for inducing intrinsic oscillations in semiconductor-based tunneling structures. Specifically, research conducted under a National Research Council (NRC) project has been used to reveal the underlying source of instability in double-barrier quantum-well structures [5]. These studies have also been used to define emitter-engineering techniques for significantly enhancing the amplitude of the oscillator current density as illustrated in Fig. 4. These oscillations have been shown to arise from subband state coupling and can therefore be characterized as a quantum fluctuation. Hence, this process immediately lends itself to the

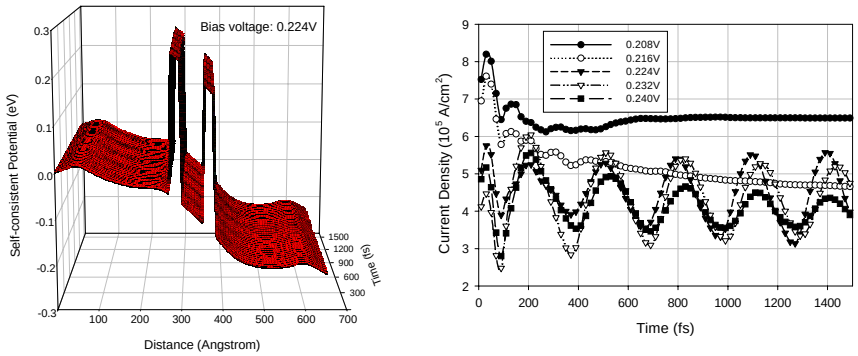

Fig. 4. *The double-barrier quantum-well structure and associated intrinsic oscillation behavior.*

design of alternative structures for generating very high-frequency oscillations. ARO also supports basic device research projects in THz electronics focused on; supperlattice-based detector and sources (UCSB), polar-optical phonon enhanced Schottky diode multipliers (UVA), Plasma-wave devices based on carbon nanotubes (UC-Irvine), Programmable molecular electronic sensors (U. of South Carolina), and an interband oscillator concept (UVA).

CONCLUSIONS The U.S. ARO has a balanced research program in THz Electronics that funds research; for making engineering advances to existing device concepts, for establishing advanced systems that can address Army & DoD relevant applications, and for defining innovative device concepts for the future. These programs are having an important impact on device and system capabilities at THz frequencies.

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Terahertz technology: generation and detection

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Abstract: This paper is reviewing recent work on sources and detectors at THz frequencies. Fundamental oscillators as well as multipliers are briefly discussed. Schottky diode doublers and triplers, heterostructure barrier varactor triplers and quintuplers are discussed. Mixers based on superconducting devices are touched upon. It is pointed out that quantum noise becomes significant at THz frequencies.

Introduction

Terahertz technology, defined as technology using frequencies from about 300 GHz to about 3 THz, will eventually become mature and used in many applications. Applications to day we find mainly in science and in particular in radio astronomy. Potential applications are expected in e.g. communications, short-range high-resolution radar systems, medical and biological imaging, high speed inter-satellite communication, earth environment monitoring, high speed wireless networks. For such applications we need reasonably cheep, lightweight and compact sources and detectors.

Available to day are backward wave oscillators (BWO) that can produce of the order a few mW to 1.5 THz, and optically pumped lasers for spot frequencies between .5 and at least 5 THz with mW output power. However, the BWO needs a heavy and bulky magnet and the laser is even more bulky and heavy. Concerning detectors and receivers, in particular radio astronomers have asked for quantum limited schemes. No amplifiers are available in this frequency range, why mixer receivers or direct detection is the only possibility. In this paper we will present ideas and results on other means of producing RF power at THz frequencies and discuss mixers. The quantum cascade laser is an interesting future THz source [20]. To day it needs cryogenic cooling and works only above ≈4 THz.

Among successful THz systems can be mentioned Odin, a recent Swedish, Canadian, Finnish and French spacecraft that was launched in February 2001 [1]. Odin has a 1.1 metre diameter telescope with tuneable heterodyne receivers covering the ranges 486 - 504 GHz and 541 - 581 GHz, and one fixed tuned low noise amplifier for 118 GHz. A more ambitious project is the ESA Herschel observatory, which will carry heterodyne receivers for frequencies between 0.48 and 1.92 THz. The launch is planned to 2007. Other projects with advanced sub-millimetre technology involved are Sofia and Planck [2].

Amplifiers

So far there are no THz amplifiers available why the heterodyne receiver is the only available option if recovery of phase and frequency information is of importance. Amplifiers to 200 GHz have been realized using HEMT transistors based on InP/InGaAs technology [3]. At 200 GHz the noise performance is poor. However, at around 100 GHz using power combining technique amplifiers with as much as 200 mW output power have been demonstrated [4]. Such high power amplifiers are very useful to drive multiplier chains delivering power at THz frequencies.

Diode Sub-mm Wave Power Sources

InP Gunn devices are compact and powerful RF sources at millimetre and possibly sub-millimetre wave frequencies. Present state of the art is about one mW at 300 GHz [5]. It is possible that mW performance of InP Gunn devices can be expected up to more than 400 GHz by optimization of device structures and circuits. The IMPATT diode is a well known transit time device. Power of almost 10 mW has been obtained near 300 GHz. The TUNNET (Tunnel Injection Transit-Time) diode is a relative of the IMPATT diode, having some advantageous for use at frequencies above 200 GHz. TUNNET diodes and novel heterostructures for frequencies above 400 GHz may play a role in the future. So far the TUNETT diode has delivered a few mW output power at around 250 GHz. For a review see ref. [5].

Single Diode Multipliers

In most practical multipliers for frequencies at about one THz and higher frequencies Gunn diode oscillators or power amplifiers in the 100 GHz range are used to pump several cascaded Schottky

doublers or triplers. Although approaches using whisker contacted diodes have been successfully implemented to a few hundred GHz, this is an extremely difficult approach from mechanical reliability point of view. To realize wide bandwidth is another difficulty using the traditional whisker contacting approach. Therefore the only really realistic way to go is to try planar solutions.

Schottky diode multipliers is the work-horse for generating power at sub-millimetre waves and THz frequencies. In Fig. 1 is shown a schematic diagram of a typical millimetre wave multiplier using a crossed waveguide topology. The output waveguide is cut-off for the input signal frequency and acts as a high-pass filter. The channel between the input and output waveguide has to be cut-off for the for the output frequency. This toplogy is common also for the multipliers using symmetric devices (see below).

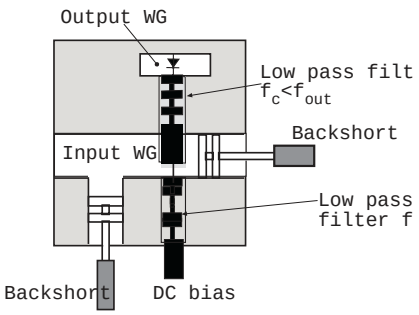


Fig. 1 Schematics of a typical single diode multiplier block using Schottky diode.

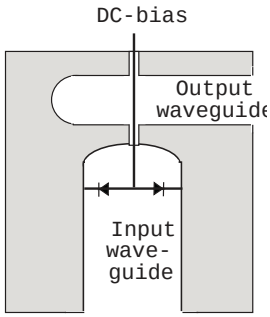


Fig. 2 THz multiplier topology [8]. *The electric field is in the plane of the figure*

A high cut-off frequency $f_c = (1/2\pi R_s)\cdot(1/C_{\min} - 1/C_{\max})$ (R_S is the series resistance, $C_{\max}$ and $C_{\min}$ the maximum and minimum capacitance during one pump period) is required for good efficiency The series resistance is obviously a key figures of merit of the devices. In order to minimize the series resistance finger shaped anodes have been patterned using electron beam lithography (see Fig 5). In addition deep etching permits one to minimize the parasitic capacitance. GaAs is used as the substrate material, and the doping of the diode is comparatively high in order to minimize electron velocity saturation effects.

Balanced frequency doublers

Balanced frequency doublers are using two Schottky diodes (see Fig. 2 and 3), and have been extremely successful for sub-millimetre wave generation. Only even harmonics are produced in this circuit, why it is ideal for a doubler. Notice that the input and output circuits have different symmetries, which is the key for understanding why only even harmonics appear in the output circuit. If in Fig. 2 and 3 one diode is reversed only odd harmonics will be generated. In this case biasing will create a problem.

At frequencies above one THz the multiplier block dimensions become so small that new approaches are necessary for implementing diodes on substrates small and thin enough. The output waveguide for e.g. a 1.5 THz multiplier should have a cut-off frequency of about 1.1 THz, i.e. the waveguide dimensions are approximately 136×68 μm. The channel where the filter between the crossed waveguides is inserted is of the order three times smaller than this. Elegant solutions have been presented for several multipliers from 200 GHz to 1.5 THz based on the schematic circuit shown

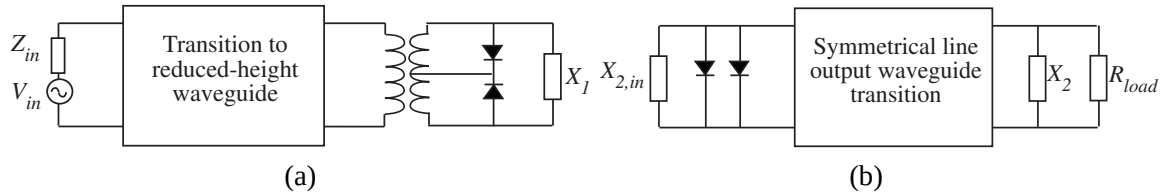


Fig. 3 Equivalent circuit of the balanced doubler of Fig. 4.3.8. (a) the input circuit, and (b) the output circuit. The various reactances are related to parasitics of the filter and waveguide structure[7].

in Fig 3. The diodes and their connections to the output waveguide, DC-bias and the grounding have been fabricated on one chip. The substrates has been reduced in thickness (down to 5 μm) or removed (partly or fully) and beam leads have been used for assuring the mechanical strength. With an input power of ≈160 mW at 100 GHz, at 400 GHz an output power of 14 mW is achieved using a "substrateless" design and cooled to 80K [8, 9]. Uncooled the power is about 75 % smaller. At 1.5

THz and at 60 K a maximum output power of 45 μW was achieved using a multiplier chain consisting of four doublers (2×2×2×2=16) [8].

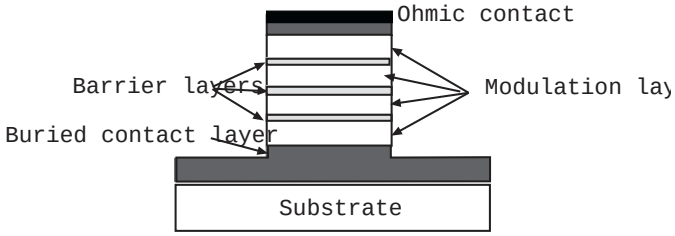


Fig. 4 Schematics of a 3-barrier HBV diode.

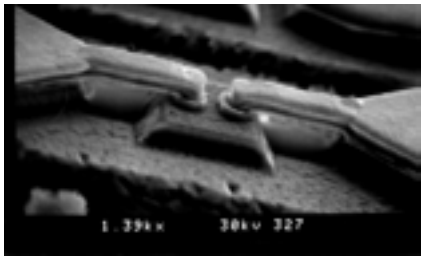
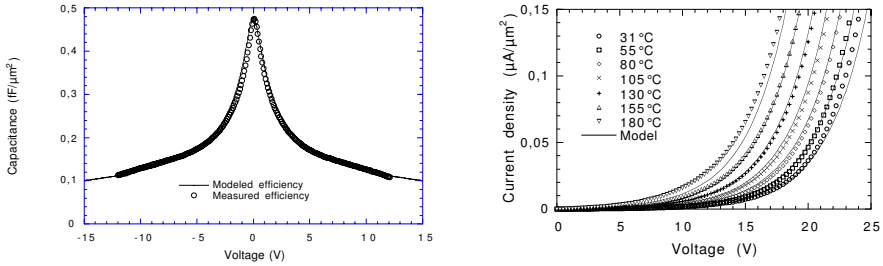


Fig. 5 SEM picture of an HBV diode. A pair of back To back Schottky diodes looks very much the same.

The Heterostructure Barrier Varactor (HBV) multiplier

A promising relative new varactor is the HBV. It is a symmetric device consisting of a high bandgap semiconductor sandwiched between two low bandgap semiconductors (Figure 4). The high bandgap material creates a barrier for electrons, i.e. it prevents electron transport through the structure. The capacitance voltage characteristic becomes symmetric (see Fig. 6a below). The structure can be grown with several barriers epitaxially stacked in series (Fig. 4) which increases the breakdown voltage and therefore also its power-handling capacity. Materials with up to 6 barriers [10] have been fabricated using state of the art material whch is based InP technology ($In_{0.53}Ga_{0.47}As/Al_{0.48}In_{0.52}As$ on InP). This material offers low leakage current and a large capacitance swing. Encouraging results have been obtained with different topologies [11, 12]. It interesting to note that even Si-SiO_x-Si [13] may prove to be a competitive materials combination.. Like for the Schottky diode multiplier resistive current causes deteriorated performance. Increased temperature of the diode obtained through self-heating consequently causes deterioration of the performance [14] (compare Fig. 6).



(a) *(b)*

Figure 6. Capacitance voltage characteristics (a) and conduction current characteristic (b) for different temperatures for a 3 barrier HBV diode.

Distributed Nonlinear Transmission Line Multipliers

A multiplier consisting of a finline loaded with 15 HBVs has been tested [15]. A finline can be used thanks to the HBVs not needing DC bias. The third harmonic is generated from propagation through the non-linear transmission line and radiated into the free space from a tapered slot antenna at the output. A maximum output power of 10 mW was generated at 130.5 GHz with an efficiency of 7%. The 3 dB bandwidth was measured to 10% and the 6 dB bandwidth to 20%.

Mixer Receivers

For frequencies below one THz SIS mixer receivers based on Nb are the outstanding mixer type [16]. Going to frequencies above one THz, losses in the SIS tuning circuit deteriorates the performance and the hot-electron bolometer (HEB) mixer takes the lead [17]. The HEB-device is quite simple. The best results until today have been obtained using a typically 400 nm long, 2 μm broad and 3.5 nm thick strip of NbN. The critical temperature of the device is about 9K. The mixing is based on the fact that the device resistance depends on temperature, which depends on power dissipation. The combination of the LO wave with the signal wave constitutes en electromagnet wave with a resulting power which is modulated with the difference IF frequency. Therefore also the temperature modulates and the bolometer resistance modulates. There is an upper IF frequency limit which set by how fast the bolometer

response is. For NbN films the –3dB fall off of the conversion gain is approximately 4 GHz. The system noise temperature achieved is 450 K at 600 GHz, 700 K at 1.6 THz and 1100 at 2.5 THz [18].

The quantum limit

The total receiver noise temperature is not far from the quantum limit (≈(optics loss)×48 K at 1 THz). Like in any receiver system the attenuation between the antenna element and the detector device is critical for reaching the ultimate performance [19].

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Impedance optimisation of millimetre-wave ASV frequency triplers

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This paper describes the design steps and experimental verification of a millimetre-wave frequency multiplier with optimised diode impedance. An anti-serial Schottky varactor (ASV) quasi-monolithically integrated into a microstrip circuit on quartz substrate is used as non-linear device for frequency tripling. Design rules for the device structure as well as for the varactor impedance are given. Experimental results show an output power of 15 mW and a flange to flange conversion efficiency of 22 % at 228 GHz.

Introduction

In order to realise local oscillators which deliver sufficient output power at upper millimetre- and submillimetre-wave frequencies, non-linear varactor diodes are used for multiplying the signal of a fundamental oscillator. The rf-circuit of frequency triplers can be simplified if varactors with symmetric characteristics are applied, since neither idler nor bias circuitry is necessary [1]. The ASV combines the advantages of symmetric devices with the low leakage currents of Schottky diodes enabling nearly pure reactive multiplication also for high amplitudes of the input signal.

Nonlinear Device

The ASV consists of two Schottky diodes with stepwise constant doping profile which are anti-serially connected by an air-bridge. This type of varactor shows a symmetric elastance-voltage characteristic and relatively low conduction currents. A large elastance change and a low series resistance are the main optimisation criteria for a high performance varactor based frequency tripler. The design rules for the individual Schottky diodes are determined by the help of a theoretical model which includes relevant physical effects such as self-biasing and maximum drift velocity of the charge carriers in the modulation zone of the varactor [2]. The resulting optimised layer sequence of the ASV for an output frequency of about 230 GHz is given in Fig. 1. The series resistance of the Schottky diodes is experimentally reduced by the help of large area n^+-contact pads [2]. Thermal limitations of the device are determined by a thermal equivalent circuit of the ASV structure on the quartz substrate. Optimisation of the varactor impedance is carried out by a further simulation programme using Fourier analysis. Since the varactor impedance increases with decreasing device diameter, small area devices are preferred for reducing circuit induced losses. However, for small area devices the output power is also small. In order to optimise the device area for a given circuit loss resistance, rf output power in dependence of the input power has been computed for different device areas. As can be seen from Fig. 2 for a given device area there exists a maximum in the output power in dependence of the input power. The envelope in Fig. 2 represents the maximum output power versus input power with device area as parameter. This correlation is shown once more in Fig. 3 where the optimum input power P_1* (for maximum output power) and the conversion efficiency are plotted versus device area. For a maximum available input power of 100 mW, for example, the optimum device area of an ASV is about of $7 \cdot 10^{-7}$ cm^2 from which a conversion efficiency of about 30 % would result (see Fig. 3).

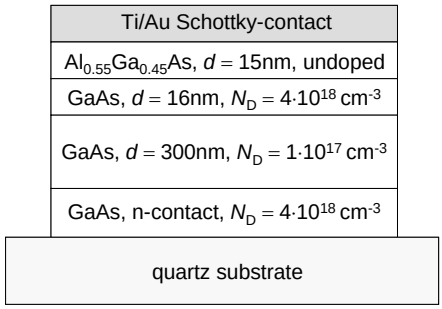

Fig. 1: *Layer sequence of a 230 GHz ASV*

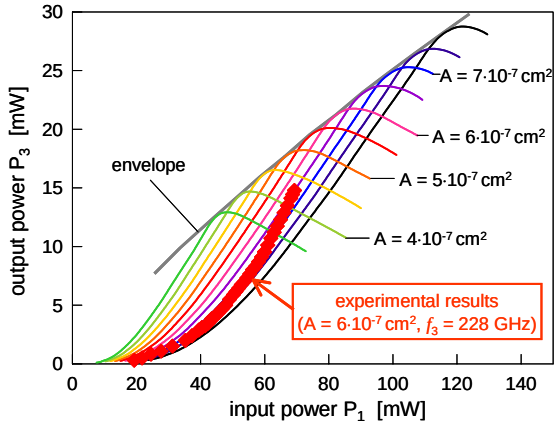

Fig. 2: *Calculated output power P_3 versus input power P_1 of ASVs with different device areas (f_1 = 76 GHz, f_3 = 228 GHz, $R_{CIRCUIT\ LOSS}$ = 0.8 Ω)*

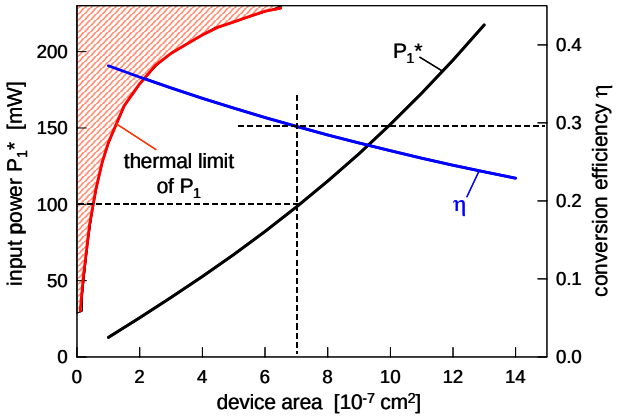

Fig. 3: *Calculated input power P_1* for maximum output power and conversion efficiency of an ASV as a function of the device area (The hatched area shows the thermal limitation of the input power)*

Tripler circuit and experimental results

The entire multiplier circuit consisting of the ASV, a low pass filter and the antennas for input and output coupling between microstrip and waveguide is fabricated quasi-monolithically integrated on quartz substrate [3]. The technique enables a combination of the low loss properties of quartz substrates with the high precision and high reproducibility of the monolithical integration. This allows an accurate control of the whole rf-circuit the design of which is performed by the help of commercial software such as HFSS and ADS. A split waveguide mount is used to test the multiplier performance of the ASV tripler circuit. Fine-tuning is realised with backshorts at both, input and output waveguide. The experimental results carried out with a device area of $6 \cdot 10^{-7}$ cm^2 led to 15 mW maximum power output (see Fig. 2) which is in good agreement with the theoretical value of 18 mW as maximum output power for the given device area. The achieved flange to flange conversion efficiency of 22 % at 228 GHz represents an essential improvement in efficiency as compared to HBV based frequency triplers [4,5].

Conclusion

Design criteria for the device structure and the impedance of a ASV frequency tripler for upper millimetre-waves are given. The optimised varactor has been fabricated quasi-monolithically integrated into a microstrip circuit on quartz substrate. The theoretically predicted tripler performance of the ASV can be confirmed with an experimentally achieved output power of 15 mW at 228 GHz with 22 % efficiency. This makes the ASV a promising candidate for mm-wave and sub-mm wave applications.

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Normal Incidence THz Wave Detection by Arrays of GaAs Lateral Single Electron Transistors

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A novel approach for normal incidence THz wave detection by planar arrays of GaAs single electron transistors (SETs) is presented. A large responsivity of 0.3 A/W was obtained for 2.5 THz at 20K.

Introduction

Intensive efforts to fill the so called "THz gap" are being made in view of applications to ultra-wide-band telecommunications, imaging and near object analysis, remote sensing, biochemistry etc. However, no solid state devices with satisfactory performance exist for generation, amplification and detection of THz signals. In this paper, a novel approach to detect THz wave by arrays of GaAs lateral single electron transistors (SETs) is presented.

Device Structure and Fabrication

The structure of the SET using Schottky wrap gates (WPGs)[1,2] is schematically shown in **Fig.1(a)**. Two nanometer-sized WPGs form double tunneling barriers and a quantum dot in between. The barrier profile and dot size/potential are controlled by the gate bias. An example of parallel integration is shown in **Fig.1(b).** For sample fabrication, GaAs nanowires were fabricated on MBE-grown AlGaAs/GaAs wafers by EB lithography and wet chemical etching. Then, Cr/Au WPGs were formed by EB lithography, metal deposition and lift-off. SEM micrographs of completed devices are shown in **Fig.2** for a single device and an integrated device having 50 SETs, respectively. Examples of the observed and calculated conductance peak are shown in **Fig.3**, confirming that current transport takes place by resonant tunneling of single electrons.[3]

THz Wave Detection

The THz response of the WPG SET devices was measured by irradiating a THz laser beam on the surfaces of devices in a normal incidence configuration, using a CH_3OH laser (2.54 THz). Measured I_D-V_G characteristics of a single dot device are shown in **Fig.4.** With THz irradiation, the conductance peak height was reduced, and a marked current increase took place at a higher gate voltages. In this case, the nanowire direction was parallel to the electric field polarization of the THz wave. When the nanowire direction was perpendicular to the polarization, no current change took place. The difference of the drain current, ΔI_D, with and without THz irradiation is also shown in **Fig.4**. The observed complicated current change could be explained quantitatively in terms of the photon assisted tunneling (PAT), using the following formula.

$$I = \frac{e^2}{h}\sum_m \int \sum_{n=-\infty}^{\infty} \frac{\Gamma_L \Gamma_R \left| J_n\left(qV_{ac}/h\nu\right)\right|^2}{\left(E - E_m + nh\nu\right)^2 + \left(\Gamma/2\right)^2}\left\{f\left(E\right) - f\left(E + qV_{DS}\right)\right\}dE \qquad (1)$$

Here, E_m is the m-th quantized state in the dot, J_n is Bessel function, V_{ac} is amplitude of ac voltage induced by THz irradiation and $h\nu$ is THz photon energy.

ΔI_D response at 2.54 THz of an integrated device having 50 SETs in parallel, measured at 20 K, is shown in **Fig.5**. Since the temperature was relatively high, only a single positive peak was induced. The responsivity of this device was high, being 0.3 A/W at 20K. Room temperature operation should be possible by further reducing the dot size and adjusting the tunneling profile and the resonance width, since the photon assisted tunneling mechanism is a energy-selective robust mechanism.

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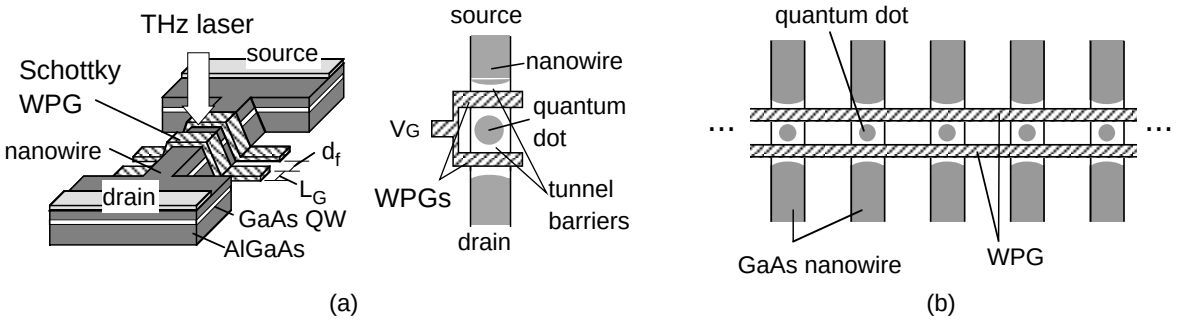

Fig.1: (a) Basic structures of WPG SET and (b) parallel SET integration.

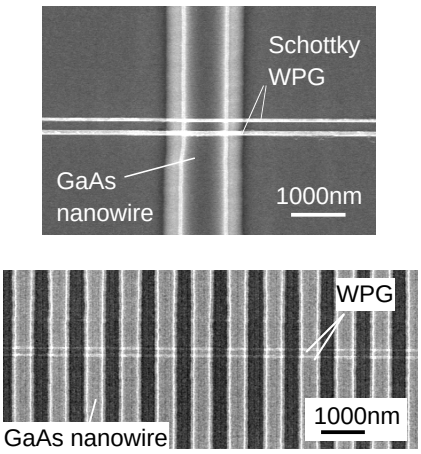

Fig. 2: SEM images of fabricated single dot SET and SET-integrated device.

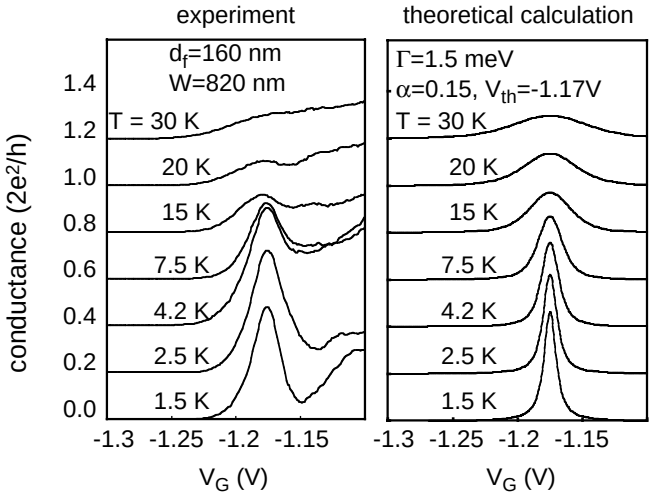

Fig.3: Conductance oscillation characteristics of a single SET.

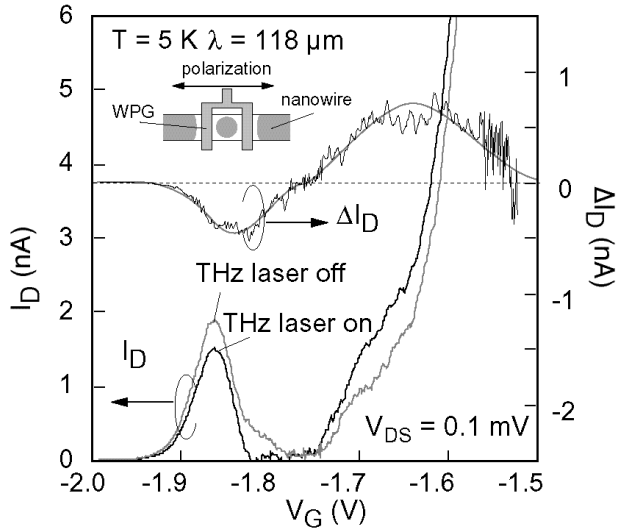

Fig. 4: Experimental I_D-V_G characteristics and ΔI_D-V_G curves.

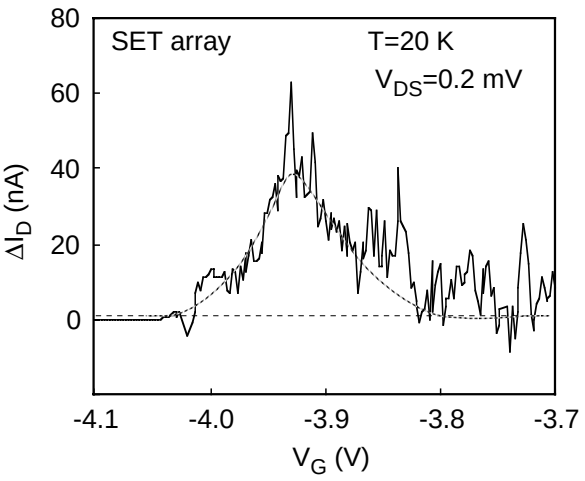

Fig. 5: ΔI_D-V_G characteristics of device integrating 50 WPG SETs in paralell.

Hybrid Modelling of Planar Heterostructure Barrier Varactors

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Abstract. Large-signal models of planar devices are derived from a combination of measurements and electromagnetic simulations. The non-linear properties of the HBV's are best characterised with microwave reflection-coefficient measurements of test structures that are essentially devoid of parasitic elements. The values of these parasitics are obtained from electromagnetic simulations of the 3D planar structure. Finally, the model is verified with measurements of the planar HBV's. The agreement between the model extracted from measurements and that obtained from electromagnetic simulations is very high.

Introduction

The fabrication of planar Heterostructure Barrier Varactors is necessary for their integration in open-structure frequency triplers for millimetric and sub-millimetric wavelengths based on coplanar waveguide or microstrip technologies. In order to integrate these devices in monolithic circuits it is necessary to develop appropriate large-signal models. The characterisation of the non-linear elements has been thoroughly studied [1] and is based on reflection-coefficient measurements. Although physical models have been successful in the representation barrier capacitance, C_{HBV}, only empirical considerations have achieved to provide accurate analytical expressions of the barrier conductance and series resistance, and therefore the use of measurement-based models of these elements remains unavoidable. The characterisation of the linear parasitic elements introduced by the auxiliary planar structure, on the contrary, can be obtained from electromagnetic simulations of the particular geometry. Thus, a modular approach to the modelling of planar devices is proposed. Its main advantage is to allow significant flexibility in the design and optimisation of planar devices.

Modelling approach

The modelling process is based in two steps. Initially a coaxial, double barrier varactor is fabricated from InP / $In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$ / AlAs epitaxial material grown at the university of Duisburg (see Figure 1.i.) This device is essentially devoid of parasitic elements and is therefore optimal for the characterisation of the intrinsic HBV's. Measurements of the reflection coefficient with a network analyser in the frequency range 500 MHz – 26.5 GHz are shown in Figure 1.ii. The use of the procedure described by Dillner and Stake provides the values of the barrier capacitance and conductance and of the series resistance at different bias voltages (see Figure 1.iii).

In a second step, the S-parameters of the planar geometry of the HBV, sketched in Figure 2.i, are calculated using a commercial electromagnetic simulator using FDTD methods [2] and further used to fit the lumped elements of the selected equivalent circuit.

The elements obtained using these two methods is finally combined substituting the parallel-plate capacitance between bridge and semiconductor material with the actual non-linear barrier. In this way a large-signal model of the two-column HBV is obtained.

Experimental Verification

In order to verify the validity of the model a coplanar HBV structure has been measured and its equivalent circuit extracted. In this process the values of the non-linear elements are taken directly as those of the coaxial structure. Table 1 compares the values of the parasitic elements obtained from the simulation with those obtained from the measurement of the planar structure. The agreement between both procedures is very high, with only one element showing a disagreement by a factor of two.

Conclusion

The modelling approach presented here, a hybrid between physical and experimental methods, represents an optimum compromise between accuracy and simplicity, which allows for flexible implementation of device-geometry optimisation. The method has been experimentally validated and may be applied to any planar device that presents significant parasitic effects introduced in the planarisation process.

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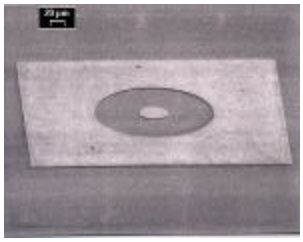
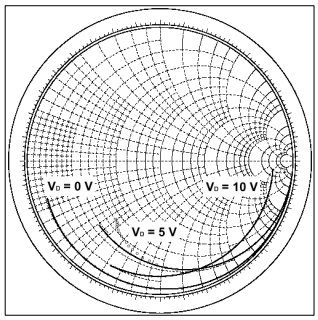


(i)

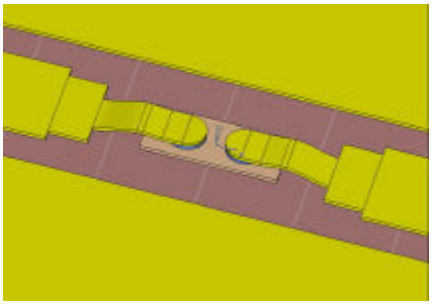


(ii)

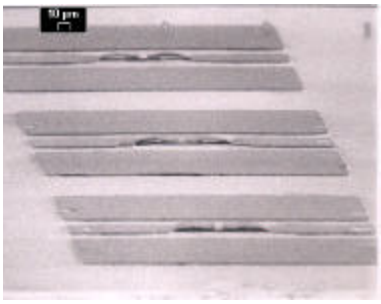
	V_D = 0 V	V_D = 5 V	V_D = 10 V
C_{HBV}	770 fF	300 fF	195 fF
R_P	$\leq 10^9$	$\approx 10^5$	625
R_S	$1.6+\frac{1.8}{1+10\,GHz/f}$	—	$3.0+\frac{0.5}{1+10\,GHz/f}$

(iii)

Figure 1: *Single-column test device with coaxial geometry for the characterisation of the non-linear properties of the epitaxial material. (i) SEM mirograph, (ii) reflection coefficient in the frequency range 500 MHz – 26.5 GHz for different bias voltages and (iii) non-linear elements of the intrinsic HBV columns obtained from coaxial structures.*

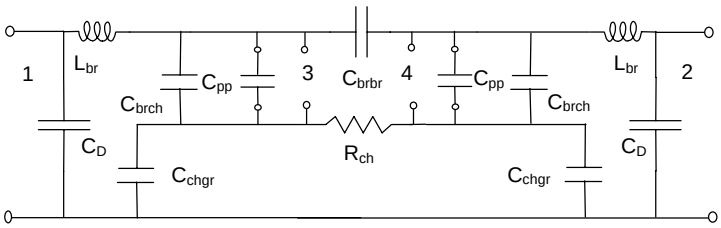


(i)



(ii)

Figure 2: *Double-column HBV with coplanar geometry used for the validation of the modelling approach. (i) Sketch of the geometry used in the electromagnetic simulation and (ii) SEM micrograph of fabricated structures.*



	Simulations	Measurements
C_D	22 fF	12 fF
L_{br}	72 pH	72 pH
C_{brch}	3 fF	3 fF
C_{chgr}	13 fF	13 fF
C_{brbr}	3 fF	3 fF
R_{ch}	2.3 Ω	2.3 Ω

Figure 3: *Compared values of the lumped elements extracted from the simulation and from the measurements of the planar structure.*